Air Force T.O. 31S5-4-308-I
Army TM 11-5805-663-14-13
Navy NAVELEX 0967-464-0010

TECHNICAL MANUAL

OPERATION AND MAINTENANCE INSTRUCTIONS

PROCESSOR ASSEMBLY (STELMA Part No. 90331023-(
AND CORE MEMORY (STELMA Part No. 90331069-(

STELMA, INCORPORATED
F19628-73-C-0014

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INTRODUCTION

The information in this technical manual pertains to Processor Assembly, STELMA Part No. 90331023-( ), and Gore Memory , STELMA Part No. 90331069-( ), hereafter referred to as Processor and Core Memory, respectively. Coverage is provided for two versions of the Processor and of the Core Memory: Processor Part No. 90331023-000 and Core Memory Part No. 90331069-600, installed in Data Analysis-Programing Group OL-122/G & ( ), hereafter referred to as Switch Group; and Processor Part No. 90331023-001 and Core Memory Part No. 90331069-001, installed in Data Analysis-Programing Group OL-123/G & ( ), hereafter referred to as Area Communications Operations Center (ACOC) Group. Because of the commonality of the two versions, and the fact that existing differences are minor, references in this technical manual to Processor and Core Memory apply to both versions; existing differences are distinguished by reference to the appropriate group (i.e., Switch Processor, Switch Core Memory, ACOC Processor, ACOC Core Memory).

The Processor, operating under program control, initiates real time data processing instructions for the Switch and ACOC Groups. The Core Memory provides word memory for storing Processor operating programs and data base information.

This technical manual, which provides information for operating and maintenance personnel, is divided into six chapters as follows;

Chapter 1, General Information, defines the purpose of the equipment and provides a brief description of, and pertinent data for, the equipment.

Chapter 2, Installation, contains procedures for unpacking and installing the equipment.

Chapter 3, Preparation for Use and Reshipment, provides procedures for initializing the equipment prior to making it operational, and preparing it for reshipment.

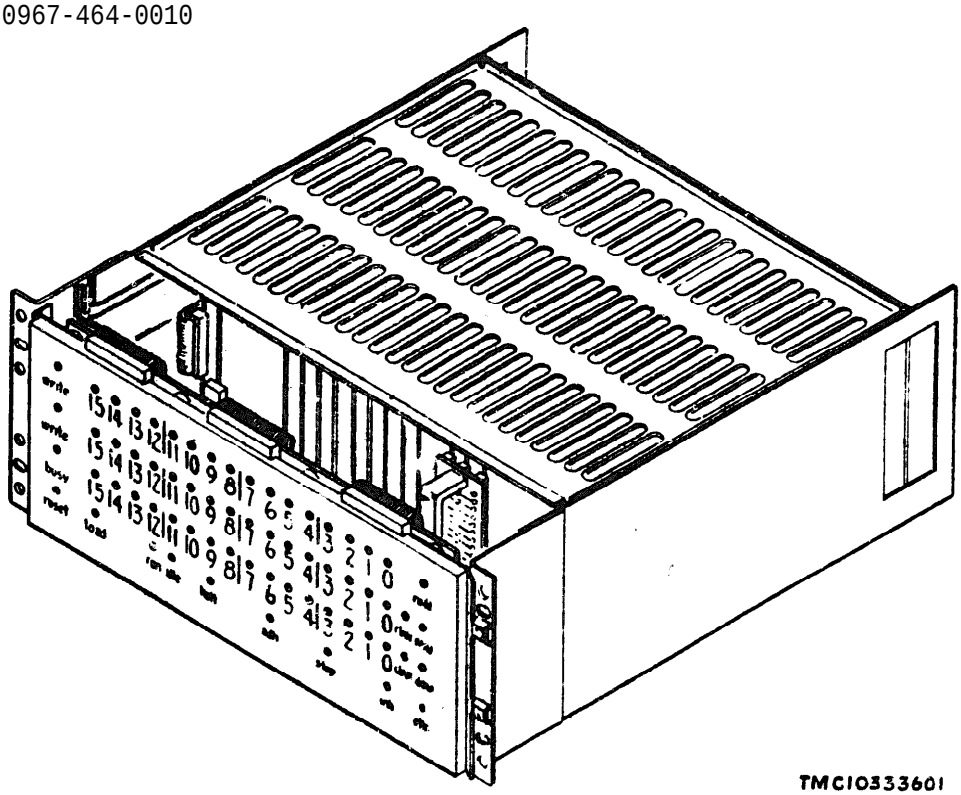
Chapter 4, Operation, contains descriptions of all controls and indicators, normal operating procedures and emergency operating procedures.

Chapter 5, Theory of Operation, discusses the functional operation of the equipment and provides descriptions of its electronic circuits.

Chapter 6, Maintenance, contains performance test data, alignment procedures, and servicing information for the equipment.

The following specifications were used in preparation of this manual.

MIL-M-38798	Manuals, Technical: Operation Instructions, Maintenance Instructions, Circuit Diagrams, Alignment Procedures, and Installation Planning
MIL-M-38784	Technical Manuals: General Requirement for Preparation of
MIL-STD-12B	Abbreviations for Use on Drawings and in Technical Type Publications
ASA Y32.16-1965	Electrical and Electronic Reference Designations
MIL-P-38790	Printed Production of Technical Manuals: General Requirements For



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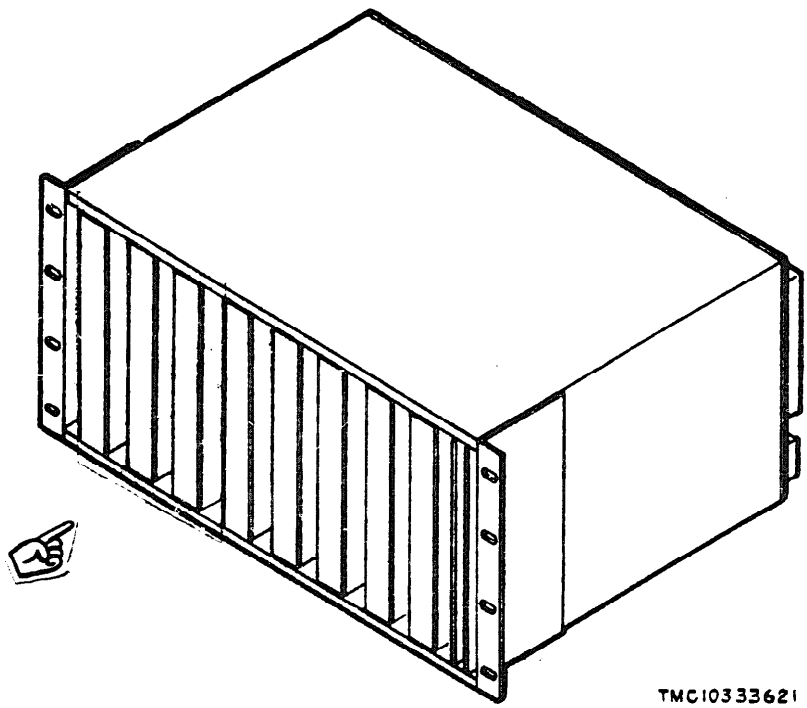

CORE MEMORY, PART NO. 90331069

Figure 1-1. Processor and Core Memory

CHAPTER 1

GENERAL INFORMATION

1-1. DESCRIPTION AND PURPOSE.

1-2. PURPOSE AND USE. The Processor (see figure 1-1) is a modified general purpose Lockheed Electronics Type SUE* mini-processor; the Core Memory (sec figure 1-1) is a modified STORE Type 333 Core Memory. Both have been modified for installation in the ACOC Group and Switch Group and to provide the following specific functions required in the Traffic Data Collection System (TDCS).

1-3. Processor Functions.

a. Receive and edit traffic data collection instructions for transmission between Switch and ACOC groups.

b. Receive and edit traffic and call data between Switch and ACOC Groups.

C. Send traffic and call data to the appropriate output.

d. Perform other processing as required to satisfy requirements between Switch and ACOC Groups.

e. Select and run programs to perform the processing automatically at the request of the Operator or Executive.

f. Provide for modifying, adding, or deleting programs.

g. Update the System clock or those portions thereof that are provided by software.

h. Provide Operator interrupt and abort capabilities and automatic interrupt capabilities for processing programs.

i. Service all input and output requests.

*System Use- Engineered

j. Respond to Operator and Switch or ACOC Groups requests for service.

k. Perform other control functions as required.

1-4. Core Memory Functions.

a. Store traffic data collection instructions for transmission and transmits them when requested.

b. Store special request traffic data collection (short) reports until the printer is available.

C. Transmit stored special request traffic data collection (short) reports to printer when requested.

1-5. The functional relationship of the Processor and Core Memory to each other and to the Switch and ACOC Groups is shown in figure 1-2.

1-6. PHYSICAL DESCRIPTION. The Processor (figure 1-3) and Core Memory (figure 1-4) as shown in figure 1-1 are housed in rectangular cases that are 19 inch standard rack mounted into the Switch and ACOC Groups. Vertical cooling is provided to the Processor and Core Memory by rack fans. The Core Memory is also horizontally cooled by three self contained exhaust fans to meet its cooling requirements. The Processor and Core Memory are interconnected by a single cable.

1-7. The Switch Processor contains 17 PC cards and the ACOC Processor contains 14 PC cards which collectively per-form the processing functions. Tire cards are inserted into an INPIBUS, a time shared data highway used as a communication

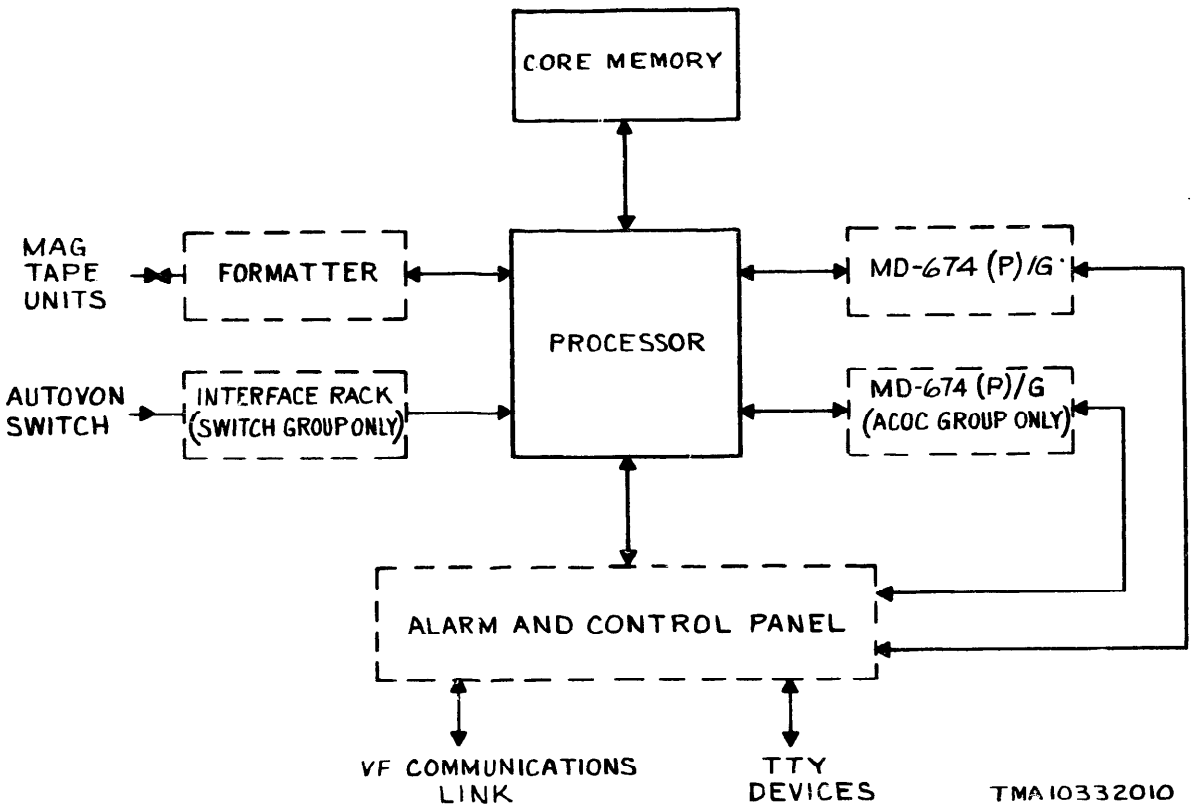

Figure 1-2. Processor and Core Memory Block Diagram

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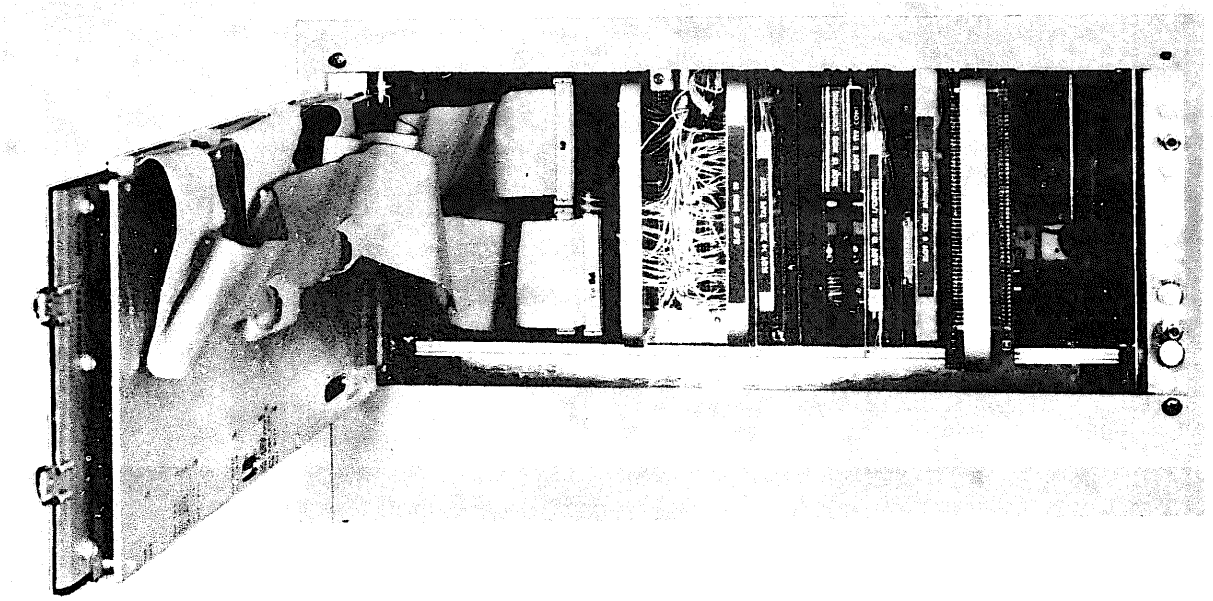

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Acoc GROUP (90331023-001)

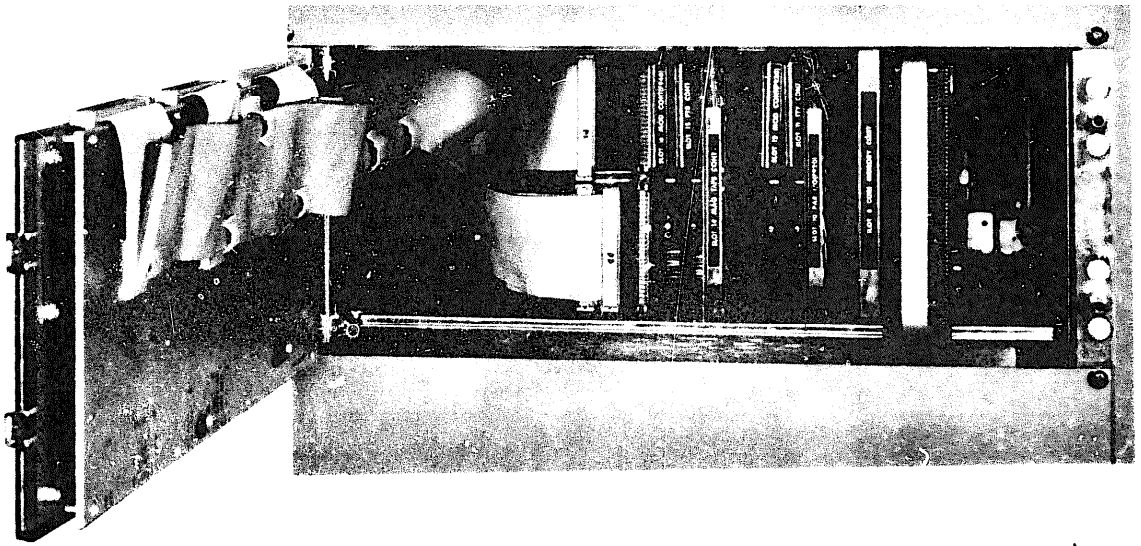

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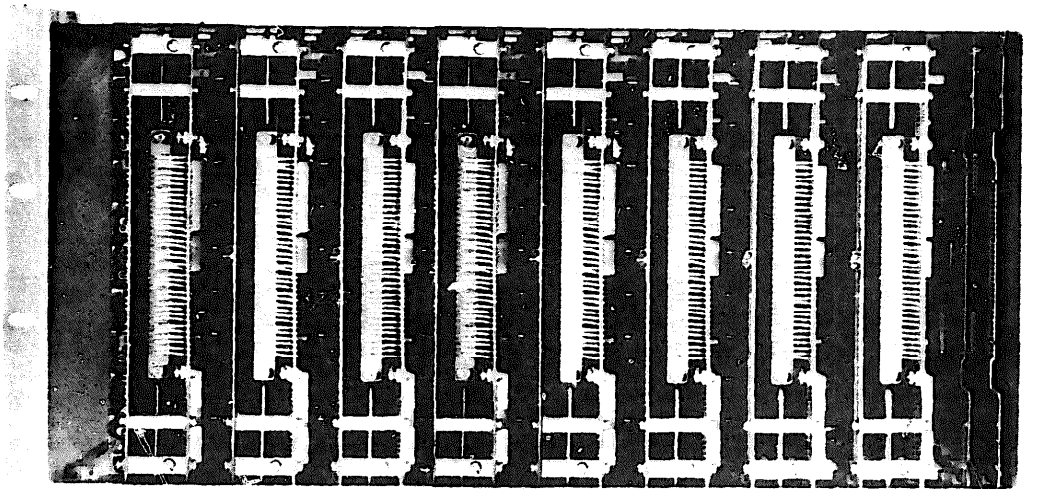
Figure 1-3. Processor, Interior View

SWITCH GROUP (90331069-000)



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ACOC GROUP (90331069-001)

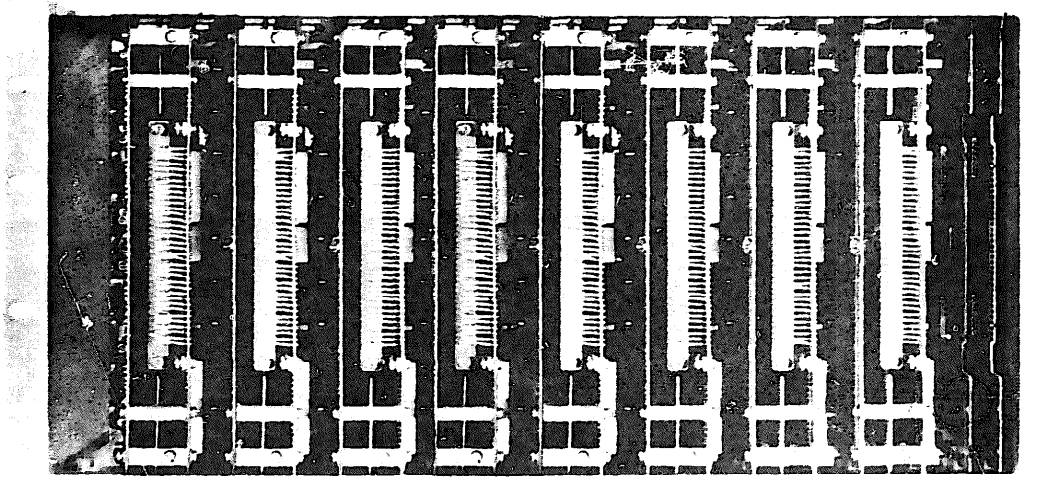

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Figure 1-4. Core Memory Interior View

link between the central processor and all other peripheral devices associated with the processor. External and other internal signals are connected to the other side of some PC cards by connectors. Mounted on the front of the Processor is a Program Maintenance Panel covered by a translucent RFI bezel. Touch-sensitive switches and light-emitting diode (LED) indicators on the panel enable a programmer or maintenance technician to check the operation of the Processor by manually entering instructions and observing readouts on the indicators. The panel is connected to the Processor by three ribbon cables.

1-8. The Switch Core Memory contains two logic control PC cards and eight magnetic core memory modules that provide 8,192 words of storage each. Thus, the Sketch Core Memory has a 65,536 word capacity (16-bits per word + 2 parity bits). The ACOC Core Memory has the same capacity as the SSU. Magnetic core memory modules are made up of three PC cards arranged in sandwich fashion and interconnected by means of standard PC board edge-connector. A terminal strip and three connectors are installed on the back cover for Core Memory power and signal interface.

1-9. The reference designation of the Processor is A1A3 and the Core Memory is A1A8. This designation is derived from the reference designation of the Data Processing Assembly Al which is a part of the Switch and ACOC Groups. The Processor is the third unit and the Core Memory is the eighth unit of this assembly. The second card of the Processor has the reference designation A1A3A2 etc.

1-10. LEADING PARTICULARS .

1-11. Table l-l lists leading particulars and logistical characteristics of the Processor and Core Memory.

1-12. CAPABILITIES AND LIMITATIONS.

1-13. Table 1-2 lists the capabilities and limitations of the Processor and Core Memory.

Table 1-1. Leading Particulars

ITEM	DESCRIPTION
Cooling:	
Processor	Vertical
Core Memory	Vertical and horizontal
Dimensions (inches):	
Processor	7 high by 19 wide by 19 deep
Core Memory	8-3/4 high by 18-1/4 wide by 15-3/4 deep
Power Requirements:	
AC:	
Processor	115 + 10 volt, single phase 50 or 60 Hz

Table 1-1. Leading Particulars (Cont'd)

ITEM	DESCRIPTION
Power Requirements: (Cont'd)	
DC:	
Processor	+5 +2% volts at 30 amperes +15 +1% volts at 1.5 amperes -15 +1% volts at 1 amperes
Switch Core Memory	+5 +3% volts at 8.0 amperes -15 +2% volts at 5.4 amperes
ACOC Core Memory	+5 +3% volts at 5.6 amperes -15 +2% volts at 4.7 amperes
Signal Cable Requirements	3 twisted pair No. 22 AWG
Storage Environment:	
Temperature	-40° to 140°F
Relative Humidity	90 percent maximum
Altitude	Sea level to 40,000 feet
Weight (pounds):	
Processor	42.0
Core Memory	46.5

Table 1-2. Capabilities and Limitations

ITEM	DESCRIPTION
Processor Capabilities:	
Data Word	16 bit
Parallel Arithmetic Register	16 bit unit that processes two register operands in 160 nano-seconds.
Registers	7 general registers available as accumulators, index registers, address pointers, stack pointers, save restore and one program counter register

Table 1-2. Capabilities and Limitations (Cont'd)

ITEM	DESCRIPTION
Processor Capabilities: (Cont'd)	
Instructions	543: 492 general register 26 branch 8 shift 17 control
Addressing	Source, target, byte and word
Bytes	65,536
Direct	Indexed, auto-increment and auto-decrement
Indirect	Indirect through index, auto-increment and auto-decrement
Programmable Shifts	Fast bit multiple positions
Branch conditions	12, either true or false
Instruction Fetch	Look-a -head
Status Indicator	Loop complete
Testing	Automatic testing of every arithmetic, logical, and move instruction for zero, negative, and add without a separate test instruction.
Auto-Increment and Auto-Decrement	In both word and byte modes
Processing	Concurrent with direct memory transfers.
Priority Interrupts	4 levels standard with unlimited sharing on levels.
Save and Store	Automatic save and restore of program counter and status combined with interrupt vectors.
Inhibiting	Selective interrupt.

Table 1-2. Capabilities and Limitations (Cont'd)

ITEM	DESCRIPTION
Core Memory Capabilities:	
Operating modes	Clear/Write. Read/Restore. Read/Modify/Write (split cycle). (Not used in TDCS) Read Only (half cycle). (Not used in TDCS)
Cycle time:	
Full Cycle	750 nanoseconds.
Split Cycle	950 nanoseconds.
Read Only	550 nanaoseconds.
Access Time	325 nanoseconds.
Memory type	3 wire, 3D coincident current.
Type of access	Random.
Data Storage:	
SSU Core Memory	All operating programs and data base information stored in a 65,536 maximum (16-bits per word + 2 parity bits) magnetic core memory.
ACOC Core Memory	Same as SW
Operating Environment:	
Temperature	4S° to 105°'F
Relative Humidity	90 percent maximum
Altitude	0 to 5000 feet

1-14. EQUIPMENT SUPPLIED.

1-15. Table 1-3 lists all modules supplied as part of the Processor and Core Memory; for each listed item, the manufacturer (or official) nomenclature, common name, and a brief description and purpose are provided.

1-16. SPECIAL TOOLS AND TEST EQUIPMENT.

1-17. No special tools are required for installation and service of the Processor and Core Memory. Table 1-4 lists test equipment required for installation and service. For each item listed, the type

designation, alternate type designation, common name and a brief de script ion of use are provided. Illustrations are provided for special test equipment.

1-18. RELATED TECHNICAL MANUALS.

1-19. Table 1-5 lists related technical manuals. For each item listed, the publications number, publications title, and equipment nomenclature are provided.

Table 1-3. Equipment Supplied

ITEM	SWITCH GROUP QTY.	ACOC GROUP QTY.	NOMENCLATURE	COMMON NAME	FUNCTION
1	1		Processor Assembly, STELMA Part No. 90331023-000	Switch Processor	Houses items 3 through 17 which are an integral part of the Processor. Operating under program control, the Processor initiates real time data processing instructions for the Switch Group.
2		1	Processor Assembly, STELMA Part No. 901331023-001	ACOC Processor	Houses items 3 through 14, and 16 through 19 which are an integral part of the Processor. Operating under program control, it initiates real time data processing instructions for the ACOC Group.
3	1	1	Bus Controller, STELMA Part No. 80331160-000	Bus Controller	Monitors and controls all communications occurring on the INFIBUS between Processor system modules.
4	1	1	CPU Control Processor Unit, STELMA Part No. 90331031	CPU	The CPU consists of a CPA and CPB, and in conjunction with the Bus Controller executes 16-bit or 32-bit word instructions from Core Memory and processes 16-bit operands in parallel.
5	1	1	CPB Control Board, STELMA Part No. 80331220-000	CPB	The CPB contains ROM control storage, microcode control logic and three registers of the CPU.

Table 1-3. Equipment Supplied (Cont'd)

ITEM	SWITCH GROUP QTY.	ACOC GROUP QTY.	NOMENCLATURE	COMMON NAME	FUNCTION
6	1	1	CPA Arithmetic Logic Unit, STELMA Part No. 80331230-000	CPS	The CPA contains bus access logic, multiplex, arithmetic logic and four registers of the CPU.
7	1	1	Core Memory Control, STELMA Part No. 80331010-000	Core Memory Controller	Provides interface between the Processor and Core Memory.
8	1	1	Auto Load Mag Tape, STELMA Part No. 80331150-000.	Autoload	Reprograms the Core Memory after a power failure from a program stored in its ROM's.
9	1	1	Parallel Input/Output STELMA Part No. 80331180-000	Parallel I/O	Interfaces the Processor INFIBUS with the Alarm and Control Card, CCU cards and CCU Controller cards sending and receiving alarm condition signals.
10	1	1	TTY Control, STELMA Part No. 80331140-000	TTY Controller	Interfaces the Processor INFIBUS and Alarm Control Panel Teletype Control Card to provide required control signals to teletype unit.
11	1	1	Modem Control, STELMA Part No. 80331210-000	Modem Controller 1	Interfaces the Processor INFIBUS and MD-674 (P)/G (Low Speed Modem) to send and receive vf data on the AUTOVON communications line via the Alarm and Control Panel.
12	1	1	Block Transfer Adapter, STELMA Part No. 80331120-000	Block Transfer Adapter	Controls Mag Tape Controller which transfers data blocks to and from the Core Memory and Mag Tape Units.
13	1	1	Mag Tape Controller, STELMA Part No. 80331130-030	Mag Tape Controller	Interfaces the Processor INFIBUS and Formatter Interface card to provide control of the Mag Tape Units.

Table 1-3. Equipment Supplied (Cont'd)

ITEM	SWITCH GROUP QTY.	ACOC GROUP QTY.	NOMENCLATURE	COMMON NAME	FUNCTION
14	1		Input/Output Controller, STELMA Part No. 80330090-000	I/O Controller	Provides control of the four Switch Group cards, traffic data control, CCL controller, RSJ control logic and RMR buffer control contained in the Processor.
15	1	1	Program Maintenance Control Panel, STELMA Part No. 90331036-000	Program Maintenance Panel	Provides a means of manual access and indication to all Processor internal registers for program control and maintenance.
16	1	1	Panel, Maintenance Program, SWB, STELMA Part No. 90331080-000	SWB	In conjunction with PBI and PCB (panel control logic) it provides a means of manual access and indication to all Processor internal registers for program control and maintenance.
17	1	1	PBI Pan Bus IF Control, STELMA Part No. 80331250-000	PBI	In conjunction with the PCB, the PBI forms the panel control logic which provides interface between the Program Maintenance Panel and the Processor INFIBUS. The PBI performs the timing, micro-operations, and status and access functions of the panel control logic.
18	1	1	PCB Control Panel Board, STELMA Part No. 80331260-000	PCB	In conjunction with the PBI, the PCB forms the panel control logic which provides interface between the Program Maintenance Panel and the Processor INFIBUS, The PCB performs the register, bus driver, LED driver, data and address selection functions of the panel control logic.

Table 1-3. Equipment Supplied (Cont'd)

ITEM	SWITCH GROUP QTY.	ACOC GROUP QTY.	NOMENCLATURE	COMMON NAME	FUNCTION
19		1	Printer Controller, STELMA Part No. 80331280-000	Printer Controller	Interfaces the Processor INFIBUS and Alarm and Control Panel Teletype Control Card to provide required control signals to teletype unit.
20		1	Serial I/O Module, STELMA Part No. 80331190-000	Modem Controller	Interfaces the Processor INFIBUS and MD-674(P)/G (Low Speed Modem) to send and receive vf data on the AUTOVON communications line via the Alarm and Control Panel.
21	1		Core Memory, STELMA Part No. 90331069-000	Switch Core Memory	Houses items 23 through 28 which are an integral part of the Core Memory. Provides 65,536 word memory for storing Processor operating programs and data base information (directory, traffic data, RMR data, etc.).
22		1	Core Memory, STELMA Part No. 90331069-001	ACOC Core Memory	Houses items 23 through 28 which are an integral part of the core memory. Provides 65,536 word memory for storing processor operating programs and data base information (directory, traffic data, etc)..
23	1	1	CM MIA, DATA PRODUCTS CORE MEMORIES Part No. 715208	CM MIA	Interfaces with the Processor, receiving control signals to generate internal timing signals for CM MIB, CM BSM's and its address registers.
24	1	1	CM MIB, DATA PRODUCTS CORE MEMORIES Part No. 714860	CM MIB	Contains a data register controlled by CM MIA timing and control logic to transfer data to and from the Processor and Core Memory.

Table 1-3. Equipment Supplied (Cont'd)

ITEM	SWITCH GROUP QTY.	ACOC GROUP QTY.	NOMENCLATURE	COMMON NAME	FUNCTION
25	5	3	CM BSM, DATA PRODUCTS CORE MEMORIES Part No. 714861	CM BSM	Basic storage module consisting of three cards; CM MBA, CM MSA, and CM MMA which provide an 8192 word x 16 bit memory.
26	5	3	CM MBA, DATA PRODUCTS CORE MEMORIES Part No. 714867	CM MBA	Provides interface conditioning, and control of data to and from the CM MMA.
27	5	3	CM MSA, DATA PRODUCTS CORE MEMORIES Part No. 741868	CM MSA	Provides control address decoding and regulation of CM MMA X and Y current sources.
28	5	3	CM MMA, DATA PRODUCTS CORE MEMORIES Part No. 715241	CM MMA	Consisting of an X and Y matrix, sense amplifiers, and magnetic core array it provides the basic storage for the Core Memory.

Table 1-4. Test Equipment List

TYPE DESIGNATION	ALTERNATE TYPE DESIGNATION	FIGURE NC'.	COMMON NAME	USE
AN/PS M-6	Model 260 55026		Multimeter	AC and dc voltage, current, and resistance measurements
MIL-C-9988	Model 5246L with options 01 and 06 28480		Electronic Frequency counter	Measure and adjust various time-base oscillators.
MIL-M-9996 Type J	Model 412A 28480		VTVM	Accurately measures dc voltages without loading circuit under test.
Model 547 with Type' 1A4 Plug-In 80009	Model 555 with two Type CA Plug-Ins 80009		Oscilloscope with Four-Trace Preamplifier	Waveform observations.

Table 1-4. Test Equipment List (Cont'd)

TYPE DESIGNATION	ALTERNATE TYPE DESIGNATION	FIGURE NO.	COMMON NAME	USE
Part No. 3916 05276		1-5	IC Test Clip	Provides access to pins of dual in-line IC chips for test probe connections.
Part No. 7970 14715		1-6	PC Card Extender	Provides access to components on PC cards in Data Processing Assembly Processor Nest 1A3 for maintenance and test purposes.
Part No. 7971 14715		1-7	PC Card Extractor	Enables removal of PC cards from Processor nest.
Part No. 713183-l 19790		1-8	PC Card Extractor	Enables removal of CM BSM module from Core Memory unit.
Part No. 7x092-1 19790		1-9	PC Card Extender	Provides access to components on CM MIA and CM MIB PC cards in Core Memory nest for test purposes.
Part No. 715138-1 19790		1-10	PC Card Extender	Provides access to components on CM BS M module in Core Memory nest for test purposes.
Part No. 80331730-000 96238		1-11	PC Card Extender	Provides electrical connecnections to I/O Controller PC card in Switch Group Processor nest for test purposes
Part No. 80331740-000 96238		1-12	PC Card Extender	Provides electrical connection to Bus Controller, CPA, or CPB PC cards in Processor nest for test purposes.
Part No. 90331059-000 96238		1-13	Switch Interface Tester	Disconnects Switch Group from AUTOVON Switch and simulates inputs for testing the I/O Controller PC card.
Part No. 25000002-000 96238			Switch Simulation Generation Program (SSGP) Tape	Provides operating program used in conjunction with Switch Interface Tester.

Table 1-4. Test Equipment List (Cont'd)

TYPE DESIGNATION	ALTERNATE TYPE DESIGNATION	FIGURE NO.	COMMON NAME	USE
	-	-	Acceptance Test Program (ATP) Test Tape	Provides test program used to systematically check all PC cards and functions of the Processor, including the Program Maintenance Panel. Also enables dump of Core Memory prior to loading of test programs.

Table 1-5. Related Technical Manuals

PUBLICATION NUMBER	PUBLICATION TITLE	EQUIPMENT NOMENCLATURE
T.O. 31W2-2G-271 T.M. 11-5805-663-14-2 NAVELEX 0967-463-7010	Technical Manual, Operation and Maintenance	Data Analysis-Programing Group OL-122/G & ( )
T.O. 31W2-2G-273 T.M. 11-5805-663-14-3 NAVELEX 0967-463-7020	Technical Manual, Circuit Diagrams	Data Analysis -Programing Group OL-122/G & ( )
T.O. 31W2-2G-274 T.M. 11-5805-663-14-4 NAVELEX 0967-463-7030	Technical Manual, Illustrated Parts Breakdown	Data Analysis-Programing Group OL-122/G & ( )
T.O. 31W2-2G-276WC-1 T.M. 11-5805-663-14-5 NAVELEX 0967-463-7040	Preventive Maintenance Work Cards	Data Analysis-Programing Group OL-122/G & ( )
T.O. 31W2-2G-281 T.M. 11-5805-663-14-6 NAVELEX 0967-463-8013	Technical Manual, Opera - tion and Maintenance	Data Analysis-Programing Group CL-123/G & ( )
T.O. 31W2-2G-283 T.M. 11-5805-663-14-7 NAVELEX 0967-463-8020	Technical Manual, Circuit Diagrams	Data Analysis -Programing Group OL-123/G & ( )
T.O. 31W2-2G-284 T.M. 11-5805-663-14-8 NAVELEX 0967-463-8030	Technical Manual, Illustrated Parts Breakdown	Data Analysis- Programing Group OL-123/G & ( )
T.O. 31W2-2G-286WC-1 T.M. 11-5805-663-14-9 NAVELEX 0967-463-8040	Preventive Maintenance Work Cards	Data Analysis-Programing Group OL-123/G & ( )

Table 1-5. Related Technical Manuals (Cont'd)

PUBLICATION NUMBER	PUBLICATION TITLE	EQUIPMENT NOMENCLATURE
T.O. 3185-4-308-3 T.M. 11-5805-663-14-11 NAVELEX 0967-464-0020	Technical Manual, Circuit Diagrams	Processor STELMA Part No. 90331023-000 (and -001) and Core Memory STELMA Part No. 90331069-000 (and -001)
T.O. 3185-4-308-4 T.M. 11-5805-663-14-12 NAVELEX. 0967-464-0030	Technical Manual, Illustrated Parts Breakdown	Processor STELMA Part No. 90331023-000 (and -001) and Core Memory STELMA Part No. 90331069-000 (and -001)

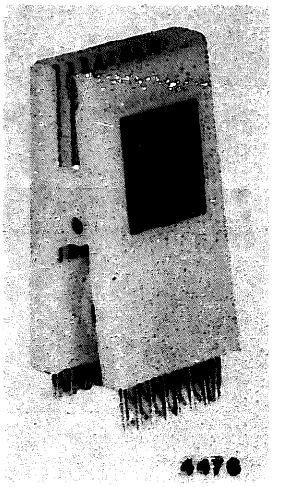


Figure 1-5. IC Test Clip, Part No. 3916

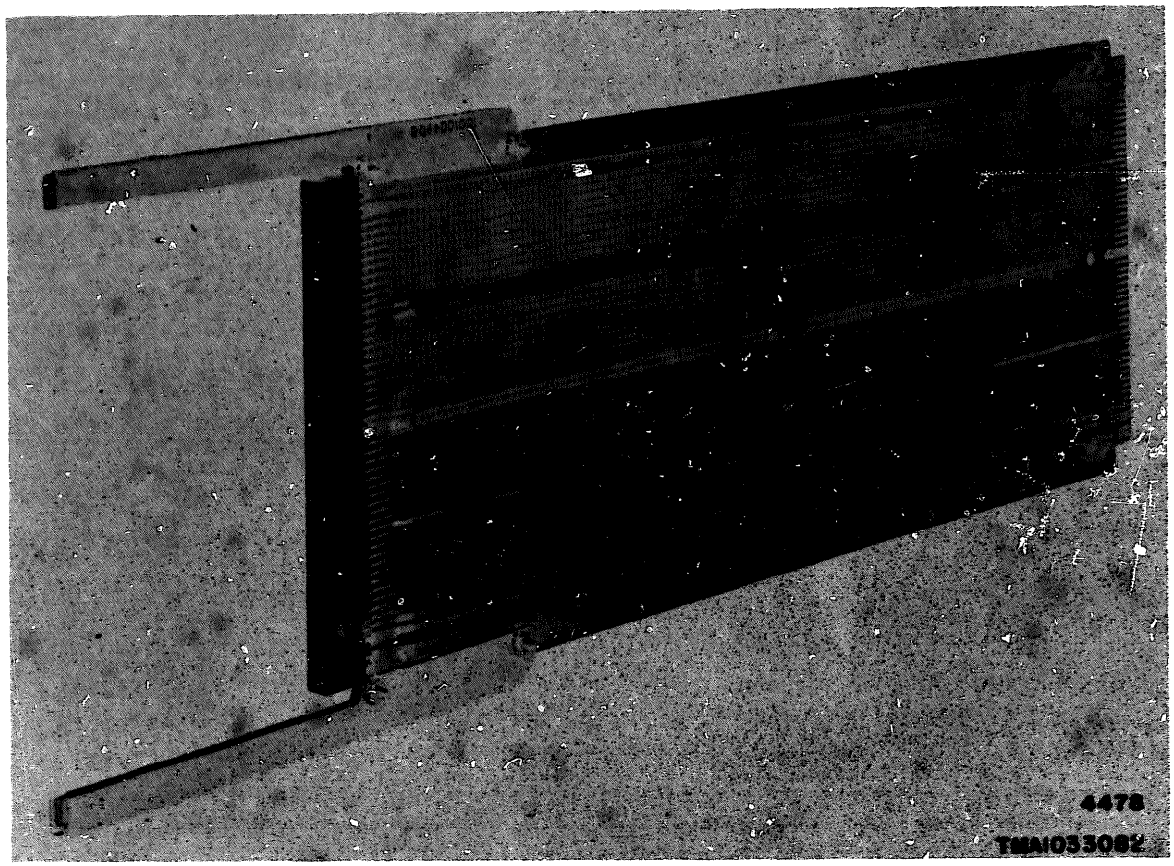


Figure 1-6. PC Card Extender, Part No. 7970

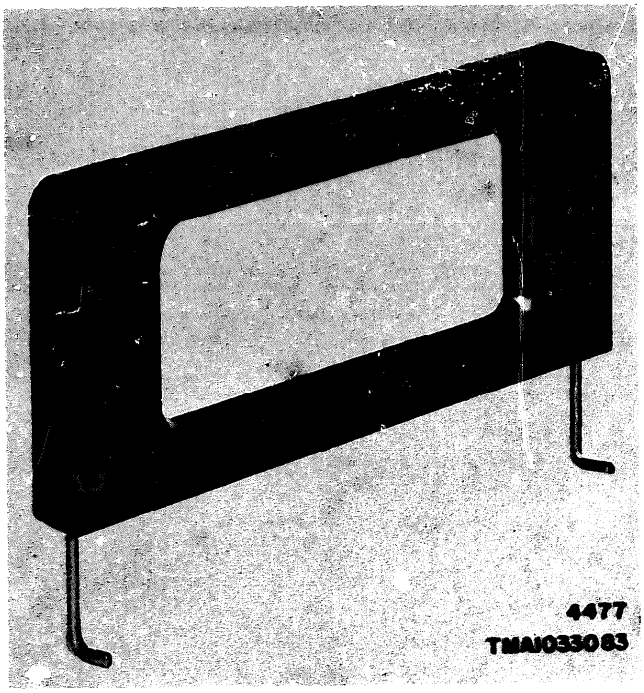


Figure 1-7. PC Card Extractor, Part No. 7971

Figure 1-8. PC Card Extractor, Part No. 713183-1

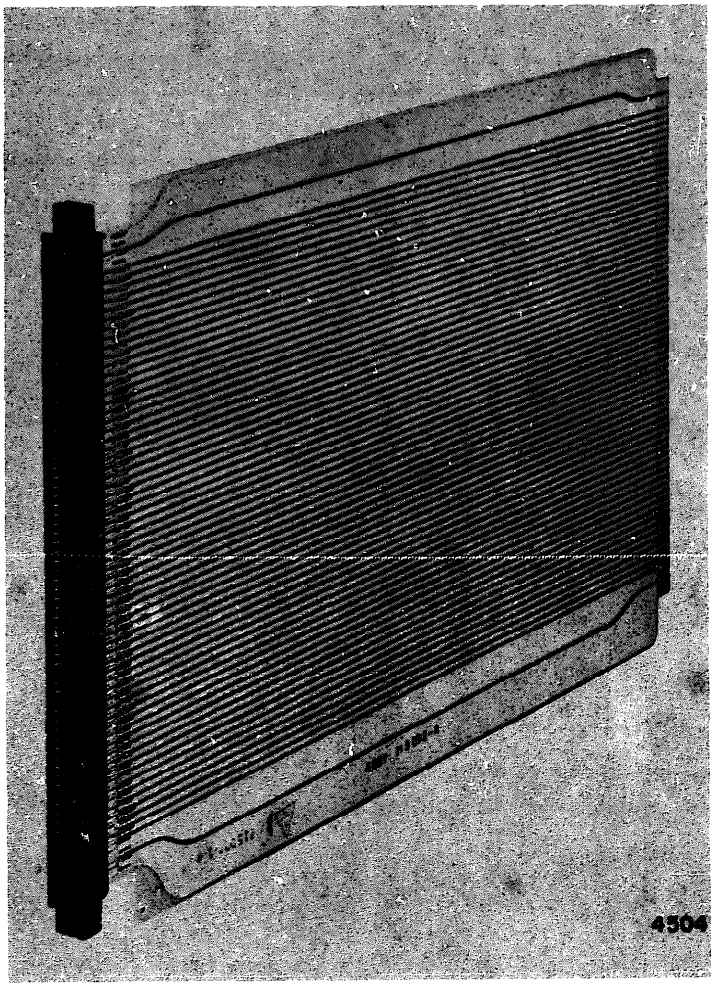


Figure 1-9. PC Card Extender, Part No. 715092-1

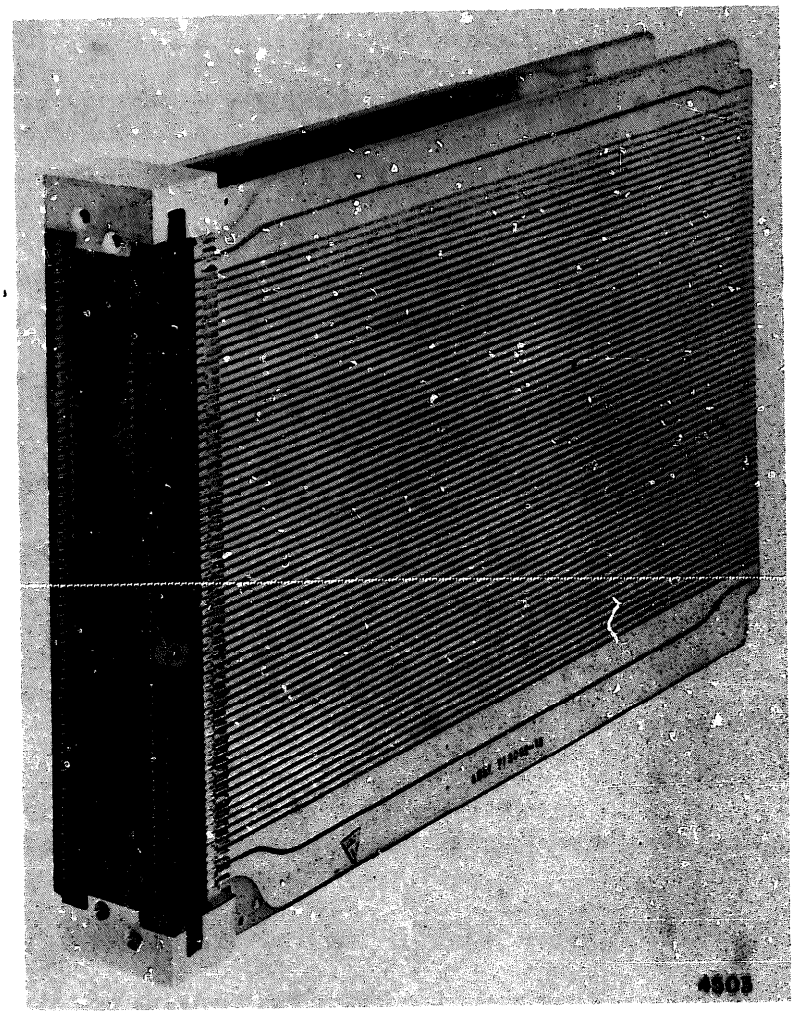


Figure 1-10. PC Card Extender, Part No. 715138-1

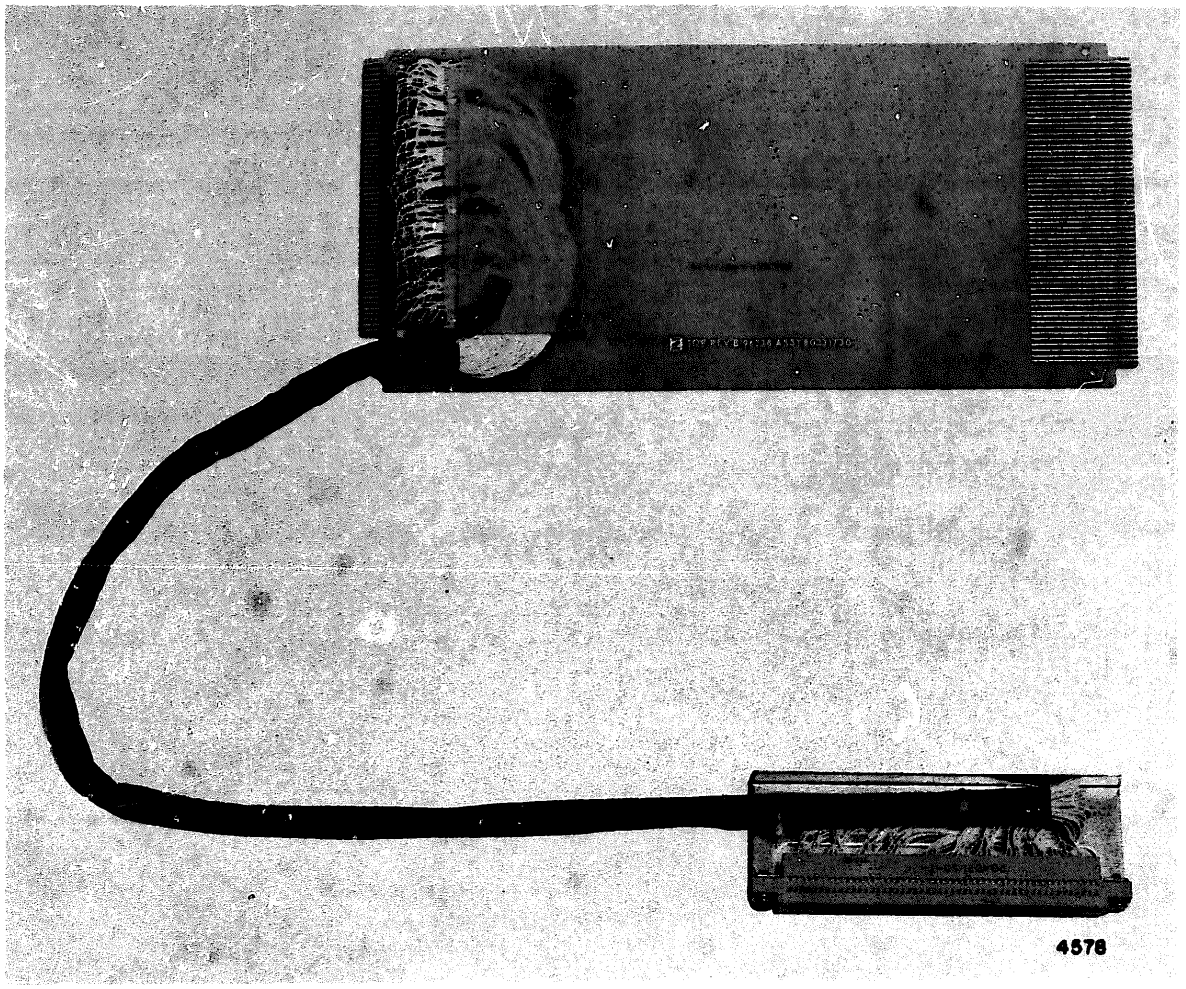


Figure 1-11. PC Card Extender, Part No. 80331730-000

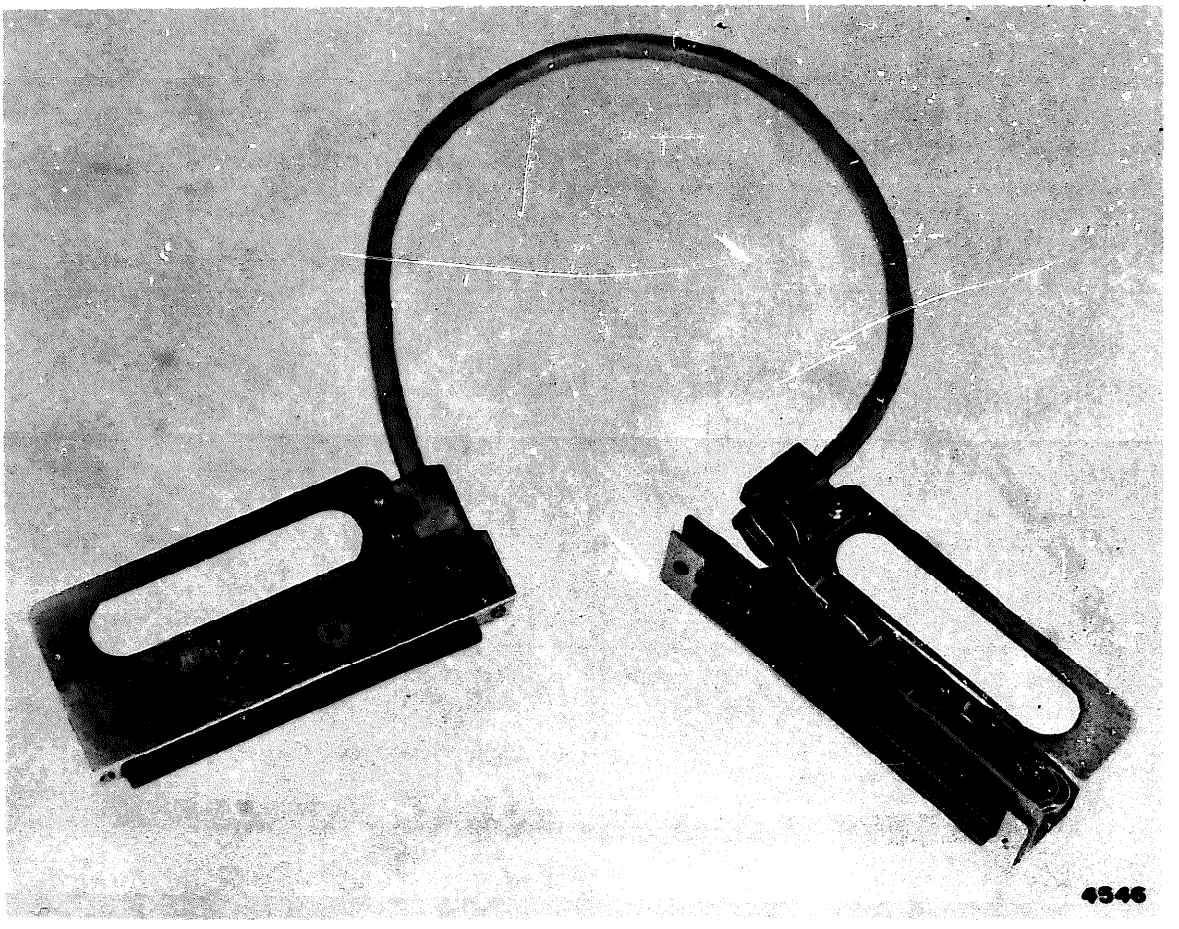


Figure 1-12. PC Card Extender, Part No. 80331740-000

Figure 1-13. Switch Interface Tester, Part No. 90331059-000

CHAPTER 2

INSTALLATION

2-1. INTRODUCTION.

2-2. This chapter contains applicable information for the installation of the Processor and Core Memory. Section I, Installation Logistics, describes: receipt and unpacking of the equipment and housing of the equipment. Section II, Installation Procedures, describes: Construction requirements, installation man-power and manhour requirements and installation sequences.

2-3. REFERENCE DATA.

2-4. The installation data contained in this section is augmented by data and instructions contained in other sections of this chapter.

SECTION I

INSTALLATION LOGISTICS

2-5. RECEIVING DATA.

2-6. Equipment packaging data for the Processor and Core Memory are described in the following group Operation and Maintenance Manuals:

1. Switch Processor and Core Memory:

   Data Analysis - Programing Group OL-122/G & ( ), T.O. 31W2-2G-271, T.M. 11-5805-663-14-2, NAVELEX 0967-463-7010

2, ACOC Processor and Core Memory:

   Data Analysis - Programing Group OL-123/G & ( ), T.O. 31W2-2G-281, T.M. 11-5805-663-14-6, NAVELEX 0967-463-8010

2-7. MATERIAL HANDLING.

2-8. The crates and boxes in which the Processor and Core Memory are packaged serve as shipping containers. For overall weights and volumes, refer to applicable group Operation and Maintenance Manual.

2-9. UNLOADING AND UNPACKING.

2-10. Unpack and check the Processor and Core Memory as described in applicable group Operation and Maintenance Manual. Save all packing materials and lists for use in the event of reshipment of the equipment.

NOTE

If equipment is damaged or incomplete, fill out and forward DD Form 6 (Report of Damage or Improper Shipment) as prescribed in AFM 75-34.

2-11. CABLING TABLES.

2-12. Interconnecting cabling information for the Processor and Core Memory is provided in the applicable group Operation and Maintenance Manual.

2-13. BUILDING AND OTHER SUPPORTING STRUCTURES.

2-14. Since the Processor and Core Memory are rack installed in their respective group, building and other supporting structures requirements are not included in this manual.

SECTION II

INSTALLATION PROCEDURES

2-15. CONSTRUCTION REQUIREMENTS.

2-16. Since the Processor and Core Memory are installed in an existing communications building, construction requirements are not included in this manual.

2-17. INSTALLATION MANPOWER AND MANHOUR REQUIREMENTS.

2-18. For installation manpower and manhour requirements of the Processor and Core Memory, refer to applicable group Operation and Maintenance Manual.

2-19. INSTALLATION SEQUENCE.

2-20. GENERAL., The work-phases described in the following paragraphs are to be performed in the given order. Before starting any procedure, carefully read through all instructions; then follow the steps in the order listed.

2-21. TOOLS AND TEST EQUIPMENT. There are no special tools or test equipment required to install the Processor and Core Memory.

2-22. PRE-INSTALLATION INSTRUCTIONS, With equipment unpacked according to instructions in paragraph 2-9, inspect equipment as described in applicable group Operation and Maintenance Manual.

2-23. MECHANICAL INSTALLATION. The Processor and Core Memory are pre-installed in the Switch and ACOC Groups without their cards and modules. For installation procedures of the cards and modules refer to applicable group Operation and Maintenance Manual. In the event the Processor and Core Memory have to be removed and installed for installation of the Switch and ACOC Groups figure 2-1 provides the dimensions of the units for rack mounting.

2-24. ELECTRICAL INSTALLATION.

2-25. POWER CONNECTIONS. Power connections are described in applicable group Circuit Diagrams Manual.

2-26. SIGNAL CONNECTIONS. Signal connections are described in applicable group Circuit Diagrams Manual.

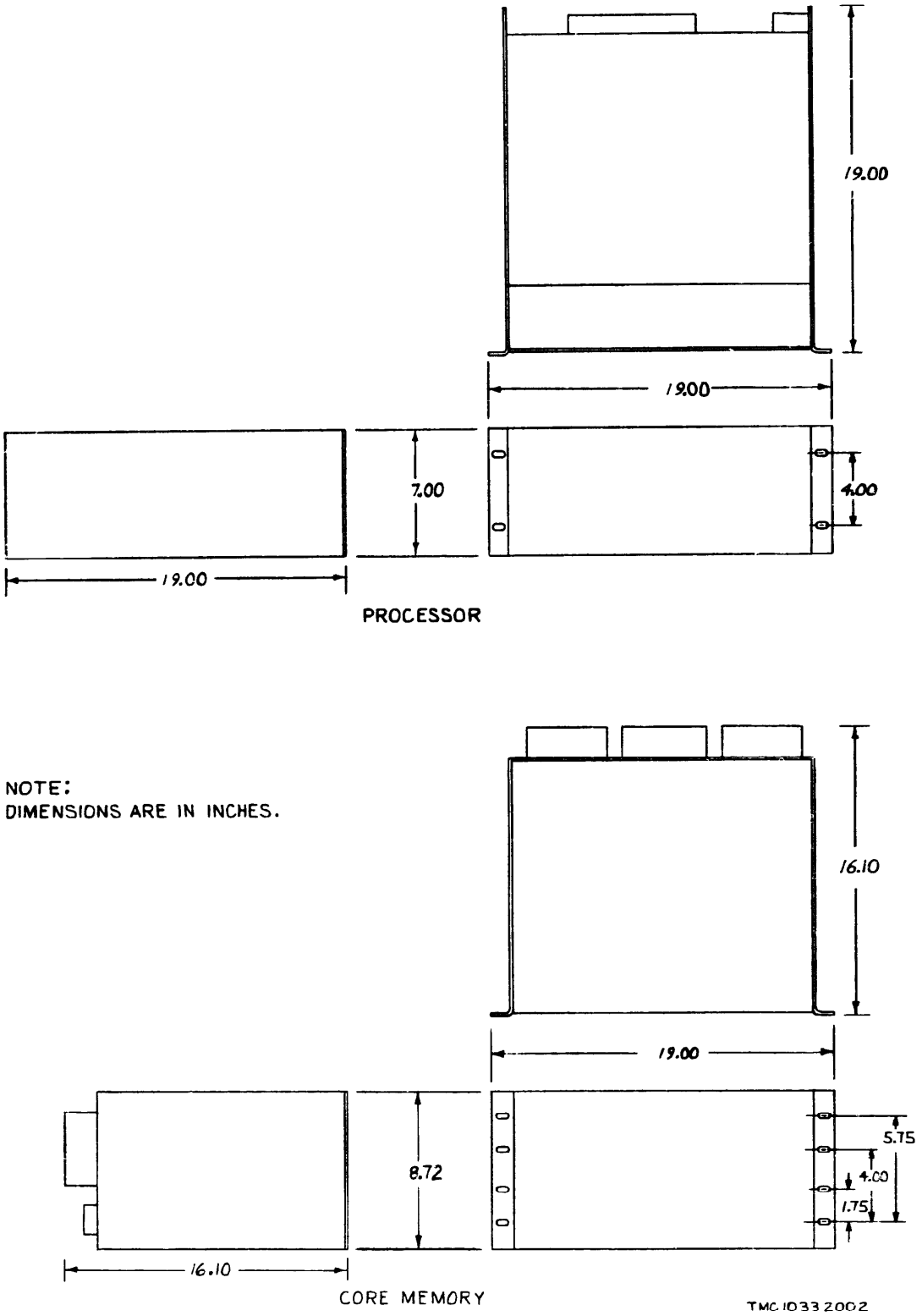


Figure 2-1. Processor and Core Memory, Outline Dimensions

CHAPTER 3

PREPARATION FOR USE AND RESHIPMENT

3-1. INTRODUCTION.

3-2. This chapter contains information applicable to preparation for use of the Processor and Core Memory. Section I describes tune-up and testing and in addition any adjustments that are required prior to equipment use. Section II describes preparation for reshipment, methods, disassembly/reassembly procedures and any special requirements to assist in reshipment.

SECTION I

PREPARATION FOR USE

3-3. The Processor and Core Memory are factory-adjusted for optimum performance and generally do not require readjustment at the time of installation. Before the Processor can be used it must be loaded with program and data base information as described in the applicable group Operation and Maintenance Manual. The units can be checked for proper operation by performing the test tabulated in Chapter 6. If readjustments are required to bring the units up to acceptable operating standards, refer to Chapter 6 for adjustment procedures.

SECTION II

PREPARATION FOR RESHIPMENT

3-4. SPECIAL INSTRUCTIONS.

3-5. To prepare the equipment for reshipment, disable it by following, in essential the reverse order, the installation procedures provided in the applicable group Operation and Maintenance Manual.

3-6. USE OF DEHYDRATING AGENT.

3-7. A dessicant agent (dehydrating agent per MIL-D-9394) should be used in the equipment crates and boxes (in lieu of water vaporproof barriers) when they are prepared for reshipment or storage. In general, 1/2-pound of dessicant should be used for every three cubic feet of crate or box.

CHAPTER 4

OPERATION

4-1. INTRODUCTION.

4-2. Operation of the Processor and Memory is an integral part of the operation of the Group in which the equipment is installed (Switch or ACOC); refer to the applicable Group Technical Manual for operating instructions and emergency operation. Section I, **Controls** and Indicators (which follows), describes the controls and indicators of the Program Maintenance Panel. Section II, Operating Instructions, and Section III, Emergency Operation, are not applicable.

SECTION I

CONTROLS AND INDICATORS

4-3. CONTROLS AND INDICATORS.

CAUTION

Do not remove the Processor protective translucent RF1 bezel and touch the switch indicators, as it will affect the data programmed into the group.

4-4. Controls and indicators for the Program Maintenance Panel are listed in table 4-1. These controls and indicators should, generally, not be touched by operating personnel unless a thorough understanding of the function of each control and indicator is obtained. The Program Maintenance Panel is primarily for use by knowledgeable programmers and maintenance personnel.

Table 4-1. Controls and Indicators (see figure 4-1)

NAME	TYPE	FUNCTION
reset	Touch response indicator switch	When touched, and while pressure remains applied, its indicator remains on and the Processor is reset. As an immediate result, the load switch indicator, the idle indicator, and the register 0 switch indicator remain on, even after reset is no longer being touched. The halt indicator is also flashed once for about 0.1 second.
load	Touch response indicator switch	The load switch is unarmed whenever its indicator is off. Unarmed, the switch remains ineffective. By touching the reset switch first, the switch is armed and becomes ready for auto-loading. Touching the switch achieves auto-loading, in which case its indicator will immediately go off. The switch is disarmed by the occurrence of any

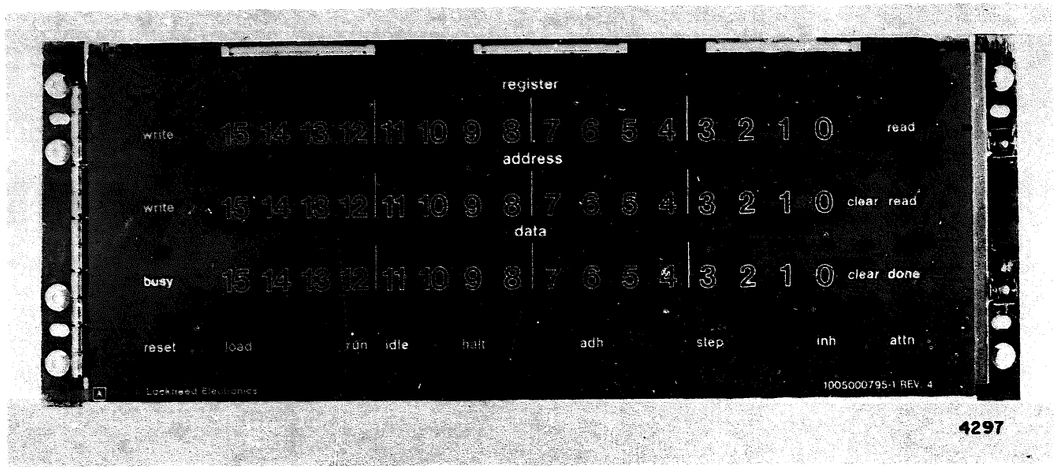


Figure 4-1. Controls and Indicators

Table 4-1. Controls and Indicators (Cont'd)

NAME	TYPE	FUNCTION
load (Cont'd)		bus transfer operation, whether initiated by the control panel, a Processor or any other system module. When power is applied to the Processor, the switch is automatically armed. The indicator goes off anytime the Program Maintenance panel is disabled, but goes on again, as soon as the Program Maintenance Panel is enabled.
inh	Touch response indicator switch	Used to inhibit all interrupts on levels 1 through 4. If the indicator goes on at the first touch, it will go out at the second touch and vice versa, giving true toggle action. The indicator, When on, indicates inhibit action.
register write	Touch response indicator switch	Touching the switch turns on its indicator, and the data displayed in the data indicators is written into the selected CPU or system Processor register. If done indicator remains on, access was successful.
register read	Touch response indicator switch	Touching the switch turns on its indicator, and, if done indicator remains on, the data indicators display the contents of the addresss CPU or system processor register.
register 0 through 15	Touch response indicator switches	Switches 0 through 15 select any one of 16 possible CPU or system processor registers. The indicator of the switch touched last is on, which represents the number of the register to be selected, and the previously on indicator is off. The following are the 16 register switches and the register they control: Switch — Register 0 — General Register 0 / Program Counter 1 — General Register 1 2 — Genera 1 Register 2 3 — General Register 3 4 — General Register 4 5 — General Register 5 6 — General Register 6 7 — General Register 7 8 — Status Register

Table 4-1. Controls and Indicators (Cont'd)

NAME	TYPE	FUNCTION
register 0 through 15 (Cont'd)		Switch / Register 9 — Instruction Register 10 — Firmware A (address of last instruction) 11 — Firmware B (operand effective address) 12 — Not assigned 13 — Not assigned 14 — Not assigned 15 — Control Register The selected register can be accessed by touching the register read or write indicator switch. Following a system reset or after power is turned on, register 0 is always selected.
address write	Touch response indicator switch	Touching the switch turns on its indicator, and the data displayed on the data indicators is written into the selected CPU or system processor address. If done indicator remains on, access was successful.
address read	Touch response indicator switch	This indicator switch operates nearly the same as the register read indicator switch, except that the data displayed in the data indicators is read at the address displayed by the address indicators. The first touch of the switch does not increment the address indicators before accessing the address. However, all following successive touches of the switch increments the address indicators by 2 before the access. Touching any other switch but the register or data switches before touching the read switch prevents the address indicators from being incremented prior to the access.
address 0 through 15	Touch response indicator switches	The address switch indicators 0 through 15 select the address to be accessed whenever the address read or write switch is touched. On indicators represent binary ONES: off they represent binary ZEROES. Each switch has toggle action, that is, if the first touch of any switch turns the indicator on, the second touch turns the indicator off, and vice versa. After touching reset or after power is turned on, the switch indicators are always cleared to 0000_{16}.

Table 4-1. Controls and Indicators (Cont'd)

NAME	TYPE	FUNCTION
address clear	Touch response indicator switch	Clears the address switch indicators to 0000_{16}.
data 0 through 15	Touch response indicator switch	The data switch indicators are used to code and generate the data to be written into the location selected by the address or register switches. The location can be in Core Memory or a selected Processor register. The switches operate the same as the address switches and the indicators are also used to display the data read from any address or register location.
data Clear	Touch response indicator switch	Clears the data switch indicators to 0000_{16}.
busy	Indicator	Indicator is on for at least 0.1 second when the INFIBUS is busy with at least one bus transfer.
done	Indicator	The indicator is on when a bus access with the Program Maintenance Panel as the master is successfully completed. In case of an abort, the indicator is off. The indicator is used only with the following switch actions: a. register write b. register read c. address write d. address read e. run f. halt g adn h. step An access by the attn switch (which accesses on external interrupt level 1 instead of on the direct data transfer level) does not use the indicator.
run	Touch response indicator switch	Touching the switch forces the CPU to resume executing instructions as long as the done indicator remains on. The indicator is on as long as the one processor is executing instructions. However, if the CPU is waiting for an external interrupt, then the idle indicator is on. After the CPU has halted program execution, the halt indicator turns on. The run and halt indicators

Table 4-1. Controls and Indicators (Cont'd)

NAME	TYPE	FUNCTION
run (Cont'd)		can appear to be on simultaneously when the run and halt conditions are interlaced at a high repetition rate. When this occurs the halt indicator could be less intense than the runindicator because the halt has a minimum delay time of 0.1 second.
idle	Indicator	The indicator is on when the CPU is waiting for an external interrupt.
halt	Touch response indicator switch	Touching the switch forces the CPU to stop executing instructions, as long as the done indicator remains on. After the CPU has halted program execution, the indicator is on.
adh	Touch response indicator switch	When indicator is on, and when the address on the INFIBUS compares exactly to the address switch indicators, the CPU is halted as long as the done indicator remains on. When the indicator is on, the switch is ineffective during the time the Program Maintenance Panel is the master accesssing the INFIBUS. The switch-indicator has toggle action.
step	Touch response indicator switch	Touching the switch turns on its indicator and causes the CPU to execute the next instruction. At the completion of this instruction the contents of the CPU register (register 15 - 0) are displayed on the data indicators. The done indicator must remain on following this action.
atten	Touch response indicator switch	This switch differs from all the others because it does not actuate until the touch is released. The indicator appears to remain off if the CPU immediately service the attention interrupt. However, if the CPU was not interrupted upon the release of the switch, then the indicator is on and the Program Maintenance Panel is locked up until the interrupt occurs. This condition occurs: a. If the CPU was halted. b. If the inh indicator has been on prior to releasing the switch. **C.** If the CPU is operating with all interrupts inhibited. The switch can always be toggled off by touching and releasing it for a second time, thereby unlocking the Program Maintenance Panel.

Table 4-1. Controls and Indicators (Cont'd)

NAME	TYPE	FUNCTION
PWR FAIL	Two-position toggle switch	In OFF position the power fail interrupt cannot be issued. In ON position the power fail interrupt is issued when the Bus Controller detects a power fail condition.
PWR RCVRY	Three-position toggle switch	Controls power recovery. In the OFF position processor is not restarted automatically, in IN position a power recovery interrupt is issued and in AL position auto-loading is achieved.
LINE FREQ	Two-position toggle switch	The line frequency interrupts are enabled when switch is ON. Line frequency interrupts are not issued if switch is OFF.

CHAPTER 5

THEORY OF OPERATION

5-1. INTRODUCTION

5-2. This chapter contains information which provides an understanding of the functional principles involved in the operation of the Processor and Core Memory. Section I describes the overall operation and tie-in of equipment. Section II describes functional operating circuit details. Section III, functional operation of mechanical assemblies, is not applicable. Illustrations referenced in this chapter are located in Technical Manual, Circuit Diagrams, T.O. 31 S5-4-308-3.

5-3. The circuits described in this chapter use positive transistor-transistor-logic (TTL) logic which may be defined in any of the following terms:

MNEMONIC-P	MNE MONIC -N
MNEMONIC	MNEMONIC
high	**low**
logic 1 to be true	logic 0 to be true
positive voltage	zero volts
open circuit	ground
	negative voltage

SECTION I

FUNCTIONAL SYSTEM OPERATION

5-4. PROCESSOR AND CORE MEMORY OVERALL BLOCK DIAGRAM DESCRIPTION.

5-5. The Processor and Core Memory (figure 1) generates and receives data and control signals to and from the Alarm Control and VF Comm Link, TTY, VF Comm Link 1, Formatter, Combiner Control Logic (CCL), Register Sender Junctor (RSJ), Rapid Memory Reload (RMR), RO TTY, and VF Comm Link 2. The Processor processes these data and control signals which are stored in or read out of the Core Memory. All operations performed by the Processor are controlled by the software program stored in in the Core Memory. The Processor also receives the Clock timing and power fail inputs from the PFD/Clock function. The clock timing signal is used to update the calendar and clock program stored in the Core Memory. The power fail input from the PFD/Clock function is used to notify the Processor of an impending power failure and causes an orderly shutdown of the Processor and Core Memory before power is removed.

5-6. Address signals, AI00-P through AILS-P determine the Core Memory address from which the data outputs, D000-P through D017-P, will be read out of; or into which the data inputs, DI00-P through DI17-P, will be written into. The DATA AVAIL-N Core Memory output notifies the Processor that the data outputs are present and ready to be transferred. The MEM AVAIL-P output from the Core Memory notifies the Processor that the Core Memory is available for further instructions. The RD INIT-P, WT INIT-P, FULL CYC-P, RD ONLY-P and MEM SEL-P outputs from the Processor determine the Core Memory mode of operation. The Core Mcmory operates in two modes; the clear/write mode and the read/restore mode. The ZW1-P and ZW2-P inputs from the Processor cause the Core **Memory to** operate in the byte mode and determine which byte of data, D000-P through D008-P or D009-P through D017-P, is to be transferred to the Processor,

5-7. PROCESSOR FUNCTIONAL BLOCK DIAGRAM DESCRIPTION.

5-8. GENERAL. The functional sections

comprising the Processor (figure 2) are as follows:

a. Bus Controller

b. CPU

c. Core Memory Controller

d. Autoload

e. Parallel I/O

f. TTY Controller

g. Modem Controller 1

h. Block Transfer Adapter

i. Mag Tape Controller

j. I/O Controller

k. Combiner Control Logic (CCL) Controller

l. Traffic Data Control

m. Register Sender Junctor (RSJ) Control Logic

n. Rapid Memory Reload (RMRj Buffer Control

o. Printer Controller

p. Modem Controller 2

q. Program Maintenance Panel.

The CCL, traffic dataa control, RSJ, and RMR functions, although physically part of the Switch Group Processor, are functionally part of the Switch Group and are therefore covered in the Switch Group technical manual (refer to table 1-5).

5-9. The Bus Controller controls the transfer to data on the INFIBUS. The INFIBUS is a common, time shared, data highway used as an asynchronous communication link between the Processor functions and external peripheral functions, The Bus Controller detects requests for INFIBUS access and when the INFIBUS is available grants INFIBUS access to the function requesting the access.

5-10. The CPU function, under control of the stored software program, performs various arithmetic and logical operations. Also, when more than one device is requesting INFIBUS access, the CPU aids the Bus Controller in resolving the priority of the access requested via the interconnect module (ICM).

5-11. The Core Memory Controller interfaces the Core Memory with the INFIBUS, controls the operation of the Core Memory and modifies INFIBUS addresses before they are applied to the Core Memory.

5-12. The Autoload function contains a fixed program that controls the operation of the Block Transfer Adapter and Mag Tape Controller when the operating program or utility print program (UPP) is being loaded into the Core Memory.

5-13. The Parallel I/O interfaces the Alarm Control and VF Comm Link with the INFIBUS and transfers bidirectional parallel bytes of data between the INFIBUS and Alarm Control and VF COMM LINK. The Parallel I/O also controls the lighting of most of the alarm and status lamps on the Alarm and Control Panel and informs the CPU of certain alarm and status conditions. In addition, the Parallel I/O controls the operation of the VF Comm Link under control of the stored software program. In the ACOC Group it also enables either VF Comm Link 1 or VF Comm Link 2.

5-14. The TTY Controller interfaces the TTY with the INFIBUS. Under control of the stored software program it converts the parallel inputs from the INFIBUS to serial output data to the TTY and converts serial input data from the TTY to parallel output data to the INFIBUS. The TTY controller also generateses and receives the control signals that allow it to send or receive data.

5-15. Modem Controller 1 interfaces the VF Comm Link 1 with the INFIBUS. Under control of the stored software program it converts the parallel inputs from the INFIBUS to serial output data to the VF Comm Link 1, and converts serial input data from the VF Comm Link 1 to parallel output data to the INFIBUS. Modem Controller 1 also gen-

erates and receives the control signals that allow it to send or receive data.

5-16. The Block Transfer Adapter controls the Mag Tape Controller during direct data transfers. A direct data transfer is a data transfer directly to or from another Processor function and IS not controlled by the CPU. The Block Transfer Adapter enables the Mag ape Controller to transfer blocks (1024 bytes) of data to and from the Formatter and the Core Memory, to and from the Formatter and RMR function, and from the Formatter to the TTY (UPP).

5-17. The Mag Tape Controller interfaces the Formatter with the INFIBUS. The Mag Tape Controller transfers bidirectional parallel bytes of data between the INFIBUS and Formatter and, under control of the stored software program, initializes the Formatter prior to data transfers.

5-18. The I/O Controller (Switch Group only) under control of the stored software program determines whether the CCL, RSJ, or RMR function has access to the INFIBUS. When the I/O Controller grants INFIBUS access to the CCL function the usage, duration and count lead information is coupled to the INFIBUS and then stored in Core Memory. When the I/O Controller grants INFIBUS access to the RSJ function, which occurs between CCL data transfers, the RSJ data is coupled to the INFIBUS and then stored in the Core Memory. When the I/O Controller grants INFIBUS access to the RMR function the bidirection RMR data is coupled between the INFIBUS and AUTOVON Switch.

5-19. The Printer Controller (ACOC Group only), interfaces the RO TTY function with the INFIBUS and, under control of the stored software program, converts the parallel inputs from the INFIBUS to serial outputs to the RO TTY function. rhe Printer Controller also generates and receives control signals that allow it to receive data.

5-20. Modem Controller 2 interfaces the VF Comm. Link 2 with the INFIBUS and, under control of the stored software program, convert s the parallel inputs from the INFIBUS to serial output data to VF Comm Link 2. It also converts serial input data from VF Comm Link 2 to parallel output data to the INFIBUS. In addition, Modem Controller 2 generates and receives control signals that allow it to send or receive data.

5-21. The Program Maintenance Panel enables a programmer to gain access to the INFIBUS manually and perform read or write operations with the Processor functions.

5-22. The INFIBUS receives a 40 msec clock signal and 9.6 KHZ power fail signal from the PFD/Clock function. The 40 msec clock signal is used to update the software calendar and clock program in the Core Memory. The 9.6 KHZ power fail signal causes the Processor to shutdown in an orderly sequence before the power being applied to the Processor and Core Memory is removed.

5-23. Master Processor functions can request INFIBUS access and, when granted service, cause another Processor function to receive or transmit data. The masters in the Processor are the CPU, Autoload, Block Transfer Adapter and Mag Tape Controller, the I/O Controller when it is operating with the CCL or RSJ functions, and the Program Maintenance Panel. Processor functions that can receive or transmit data only when addressed are called slaves. The slaves in the Processor are the Core Memory Controller, Parallel I/O: TTY Controller, Modem Controller 1, Mag Tape Controller, I/O Controller (while operating with the RMR function), Printer Controller, and Modem Controller 2. A master can also operate as a slave when addressed by another master.

5-24. Addresses are 16-bit hexadecimal words placed on the INFIBUS by the master to select the desired slave. Addresses in the range of 000016 through OOFFI6 are used by the CPU while handling interrupts and to vector to the appropriate subroutine in the stored software program. This range of **addresses** is referred to as the executive **space** of the Core Memory. Addresses from 0100 16 through DFFF 16 are assigned to the operating programs and data storage

dress in the range of FOOO 16 through FFFF 16 is assigned to each Processor function with the exception of the Bus Controller. Each Processor slave is capable of recognizing its assigned address when it is on the INFIBUS. Each slave is also capable of placing its address on the INFIBUS data lines when it is requesting INFIBUS access.

5-25. Each Processor function has three basic registers; the data register, control register, and status register. Each of these registers can be selected (addressed) by a master. The register that is to be selected is determined by the value of the 4 least significant bits of the 16-bit address. The data register is usually comprised of two registers, one which provides data from the INFIBUS to the external function and one which provides data from the external function to the INFIBUS. The control register stores command words issued by the stored software program which'start and stop function operations. The status register indicates to the CPU that the Processor function and external device are ready and indicates any errors detected in the operation of the external device. Also, writing into the status register causes that function to be cleared.

5-26. BUS CONTROLLER. All communications between Processor functions are via the INFIBUS which is controlled by the Bus Controller. Communications on the INFIBUS are asynchronous 'and bidirectional- (one direction at a time). All communications between Processor functions consist of two cycles, first the select cycle then the service cycle. The primary purpose of the Bus Controller is to allocate INFIBUS time to Processor functions on a priority basis. The secondary function of the Bus Controller is to generate CFU internal interrupts for power fail, power restart, calendar and clock stored software program update, and operator attention.

5-27. During the select cycle, a Processor function requests INFIBUS access and then the Bus Controller, depending on the priority of the request, grants INFIBUS access to the Processor function. When the Processor function gains access to the INFIBUS, the Processor function service cycle begins. During the service cycle the Processor function transfers the information to the INFIBUS. These request and service cycles can overlap in time. While one function is performing a service cycle another function may be performing a request cycle and when the first function completes its service cycle the second function then performs its service cycle.

5-28. Requests for INFIBUS access are received by the Bus Controller on service request lines which are assigned priority levels according to their communication function. There are three types of communication priorities; module selection and service, interrupt selection and service, and CPU selection and service.

5-29. Module selection and service occurs when a Processor master requires the INFIBUS to perform a data transfer directly to or from the Core Memory or other Processor functions. These data transfers are referred to as direct data transfers (DDT) and are not under control of the CPU and stored software program. DDT transfers are the highest priority level transfers and take precedence over all other requests for INFIBUS access. The SRLD-N request line is activated when a DDT is requested.

5-30. Interrupt selection and service occurs on one of four assigned priority levels when a Processor function requires the INFIBUS to perform a data transfer under control of the CPU and stored software program. The four interrupt request lines, SRL4-N through SRLl-N (level 4 through level 1 interrupts), determine the priority of the interrupt requests. SRL4-N is the highest level priority interrupt request and SRL1-N is the lowest level priority Interrupt request. All DDT requests must be serviced before interrupt requests may be serviced in their order of priority.

5-31. CPU selection and service occurs when the CPU requires the INFIBUS to execute the stored software program. CPU selection and service is also a DDT request. However, these transfers on the INFIBUS have the lowest priority and the SRLC-N

request line is activated by the CPU and detected by the Bus Controller.

5-32. The precedence pulse, PCDA/B-P is chained through all functions of the Processor and determines which function (when more than ore function is requesting the INFIBUS on the same priority level) will gain INFIBUS access first. The precedence pulse is referred to as PCDB-P when generated by or exiting from a function and PCDA-P when entering a function. Assume that two functions, the Parallel I/O and TTY Controller, are requesting INFIBUS access. SRL1-N is generated by both functions and is detected by the Bus Controller. The Bus Controller generates the select line, SEL1-N, and PCDB-P. PCDA-P is coupled through and delayed by the CPU and Autoload functions and trapped by the Parallel I/O. Trapping the precedence pulse enables the Parallel I/O to gain INFIBUS access first. When the Parallel I/O completes its transfer, the Bus Controller generates PCDB-P again (SRL1 -N still being generated by TTY Controller) which is trapped by the TTY Controller. The precedence pulse serves to grant INFIBUS access to the function nearest the Bus Controller first when two or more functions are requesting INFIBUS access on the same priority level.

5-33. When one or more masters are requesting a DDT, the master or masters generate SRLD-N (waveform A, figure 3). The Bus Controller senses SRLD-N and selects SRLD-N over other requests. The Bus Controller then generates the select signal, SELD-N (waveform B, figure 3), and the precedence pulse, PCDA-P (waveform C, figure 3). SRLD-N is received by all of the masters requesting INFIBUS access but PCDA-P reaches the master nearest the Bus Controller first. This master prevents the precedence pulse from being coupled to the other masters. The master requesting the INFIBUS access now generates SACK-N (waveform D, figure 3) which notifies the Bus Controller of a successful selection and prevents other functions from requesting INFIBUS access during the time it is glen-- era ted. If SACK-N is not sensed by the Bus Controller within 2 microseconds after SELD-N and PCDA-P are generated, the Bus Controller generates SACK-N which will abort the selection cycle. The function requesting the INFIBUS access must then reinitiate the request.

5-34. After the selected master generates SACK-N, SRLD-N is removed. The Bus Controller senses SACK-N and the removal of SRLD-N and then removes SELD-N. The selected master monitors STRB-N and when STRB-N is removed, the address, control, and data (if a write operation) is placed on the INFIBUS. The selected master places the address on the INFIBUS address lines, AB00-N through AB15-N (waveform E, figure 3). If the master is to write data into the function being slaved (addressed), it generates RITE-N (waveform F, figure 3). If it is to read data from the function being slaved, it holds the RITE-N line high. If the data being transferred is a 16-bit word, the master holds BYTE-N high and data lines, DB00-N through DB15-N (waveform G, figure 3), are used. If the transfer is to be an 8-bit byte, the master generates BYTE-N and only 8 data lines, DB00-N through DB07-N, are used. The selected master now generates STRB-N which allows the requested data transfer to occur (service cycle) and removes SACK-N which allows the Bus Controller to select the next master if it is requesting INFIBTUS access.

5-35. If a second master is requesting INFIBUS access, the Bus Controller selects this function in the same manner it selected the first master. While the second master function is being selected, the slave (addressed) function of the first master function recognizes its address on the INFIBUS and the data is written into or the data (waveform I, figure 3) is read out of the slave. When the data transfer is complete, the slave generates DONE-N (waveform J, figure 3) which causes the first master to remove the address, control, and data (if a write operation) from the INFIBUS. Receiving DONE-N also causes the master to remove STRB-N from the INFIBUS. The second selected master function senses the removal of STRB-N and places address, control and data (if a write operation) signals on the INFIBUS and a data transfer occurs as explained for the first master. Upon comple-

tion of the data transfer, if no other function is requesting INFIBUS access, STRB-N is removed and the INFIBUS is idle. If either master does not receive DONE-N within 2 usec after STRB-N is generated, the Bus Controller generates QUIT-N which aborts the service cycle and frees the INFIBUS for other data transfers by forcing the selected master to remove STRB-N.

5-36. When a function requests a level four interrupt, it generates SRL4-N (waveform A, figure 4). The Bus Controller senses SRL4-N and generates NEXT-N (waveform B, figure 4) to the CPU through the interconnecting module (ICM). NEXT-N informs the CPU that an interrupt has been sensed and the CPU completes its current step and jumps to an interrupt stored software program subroutine. When ready to accept the interrupt, the CPU generates SCM3-N (waveform C, figure 4) to the Bus Controller via the ICM. SCM3-N allows the Bus Controller to select the interrupt if the higher priority signal SRLD-N is not being generated by a master. The Bus Controller now generates the select line, SEL4-N (waveform D, figure 4), and the precedence pulse, PCDA-P (waveform E, figure 4). The interrupting function senses SEL4-N, traps the procedence pulse, and then removes SRL4-N and generates SACK-N (waveform F, figure 4). SACK-N prevents other functions from requesting INFIBUS access and is sensed by the Bus Controller which removes SEL4-N . The Bus Controller then generates HOLD-N (waveform G, figure 4) which is routed to the CPU. HOLD-N prevents the CPU from performing any operations with the Core Memory. The Bus Controller also generates a binary code, ILOR-N and IL1R-N (waveform H, figure 4), which is routed to the CPU. This binary code informs the CPU that a level 4 interrupt has been selected.

5-37. The selected interrupting function now places its device number (waveform 1, figure 4) on the INFIBUS data lines DB04-N through DBl-N. It then generates STRB-N (waveform J, figure 4) and removes SACK-N which allows a second interrupting function to be selected. The Bus Controller senses the generation of STRB-N and the removal of SACK-N which causes DNOL-P (waveform K, figure 4) to be generated. DNOL-P informs the CPU that the interrupting functions device number is on the INFIBUS. The CPU reads the device number from the INFIBUS and then generates DONE-N (waveform L, figure 4) to indicate the interrupt request is loaded in the CPU. After the removal of DONE-N, the interrupting function removes STRB-N which frees the INFIBUS for other operations.

5-38. Between these other INFIBUS operations, the CPU transfers the device number of the interrupting function to the level 4 area of executive space in the Core Memory. The CPU now vectors to a stored software program subroutine that accesses the interrupting function and allows data to be transferred into or out of the interrupting function. The actual sequence of events involved is determined by the stored software program.

5-39. While the device number is being processed by the CPU, the CPU generates mask bits LB12-P through LB15-P (waveform M, figure 4) which are routed to the Bus Controller. At the same time the CPU generates STAT-N (waveform N, figure 4) which strobes the mask bits into the Bus Controller. The mask bits are used to block the serviced interrupt level and allows the next lower priority interrupt level to be selected. In this way one interrupt level cannot tie up the CPU and the four levels of interrupts are each sequentially serviced. During a level 4 interrupt INFIBUS access request, the level 4 interrupt will be closed (masked) and the level 3 interrupt will be opened. When the level 3 interrupt is completed the level 2 interrupt will be serviced. When the level 2 interrupt is completed, the level 1 interrupt is serviced and when the level 1 interrupt is completed the level 4 interrupt is opened again.

5-40. When a Processor function requests a level 3 interrupt, operation is the same as a level 4 interrupt except that SRL3-N and SEL3-N are used and the Bus Controller generates a binary code (ILOR-N and IL1R-N) which represents a level 3 interrupt. Also, the CPU generates mask bits (LB12-P through LB15-P) which block the level 3 interrupt and open the level 2 interrupt.

5-41. When a Processor function requests a level 2 interrupt, operation is the same as a level 4 Interrupt except that SRL2-N and SEL2-N are used and the Bus Controller generates a binary code (ILOR-N and IL1R-N) which represents a level 2 interrupt. Also, the CPU generates mask bits (LB12-P through LB15-P) which block the level 2 interrupt and open the level 1 interrupt.

5-42. When a Processor function requests a level 1 Interrupt, operation is the same as a level 4 interrupt except that SRL1-N and SELl-N are used and the Bus Controller generates a binary code (ILOR-N and IL1R-N) which represents a level 1 interrupt. Also, the CPU generates mask bits (LB12-P through LB15-P) which block the level 1 Interrupt and open the level 4 interrupt.

5-43. If SACK-N is not sensed by the Bus Controller within 2 usec after SEL4-N, SEL3-N, SEL2-N or SEL1-N and PCDA-P is generated, the Bus Controller generates SACK-?': which will abort the associated interrupt request. If DONE-N is not generated by the CPU within 2 usec after STRB-N is generated by the interrupting function, the Bus Controller generates QUIT-N which aborts the interrupt and frees the INFIBUS.

5-44. The lowest level priority for INFIBUS access is CPU selection and service. This priority, called CPU interrupt: operates in exactly the same manner as module selection and service (DDT) except that this interrupt uses the SRLC-N and SELC-N signals rather than the SRLD-N and SELD-N signals. The CPU interrupt is also a DDT however, these transfers occur only between the CPU and the Core Memory Controller. They are generated when it is required to write data into or read data out of the Core Memory under control of the stored software program.

5-45. The secondary function of the Bus Controller is to generate CPU internal interrupts. CPU internal interrupts are generated by the Bus Controller for power fail, power restart, to update the calendar and clock program stored in the Core Memory, and for operator attention.

5-46. The PWST-N input to the Bus Controller from the PFD/CLOCK function is the power fail/power restart signal. It is a 9.6 kilohertz square wave signal that is generated 2.2 to 3.0 msec before loss of regulated dc power and it is a level 4 internal interrupts. The Bus Controller, upon sensing PWST-N, generates an internal level 4 internal interrupts to the CPU to notify it of eventual loss of power and then generates master reset pulses MRES-N. MRES-N is routed to all Processor functions to clear each function. Between these MRES-N pulses, the CPU performs required operations for an orderly shutdown. If regulation is only lost momentarily and then regained, the Bus Controller generates a second level 4 internal interrupts to notify the CPU of restored power. Associated with power fail and power restart internal Interrupts are PFIN-N, PRIN-N and PRAL-N inputs to the Bus Controller from the Program. Maintenance Panel. PFIN-N is generated by a switch behind the front panel and the Bus Controller uses PFIN-N to inhibit a power fail level 4 internal interrupts. PRIN-N and PRAL-N are generated by a three position switch located behind to inhibit the power restart level 4 internal interrupts. in the AL position, PRAL-N is generated and the Bus Controller generates autoload signal, ATLD-N, when power restart is indicated instead of the level 4 internal interrupts. In the OFF position, the level 4 internal interrupts is enabled and ATLD-N is inhibited.

5-47. The LFRQ-N input to the Bus Controller is a pulse generated every 40 msec by the PFD/Clock function. The Bus Controller uses this pulse to also generate a level 4 internal interrputs. Every 40 msec the LFRQ-N level 4 internal interrupts causes the CPU to update the calendar and clock program stored in the Core Memory. Associated with LFRQ-N is the LFIN-N input from the Program Maintenance Panel which is generated by a switch located behind the front panel. LFIN-N inhibits the LFRQ-N level 4 internal interrupts.

5-48. The EXAT-N **input is generated** by the Program m Maintenance Pane! when the

attention (attn) switch on the front panel IS depressed. This causes the Bus Controller to generate a level 1 internal interrupts to inform the CPU of a request by an operator for INFIBUS access. Not used in TCDS.

5-49 . The power fall, power restart, and software clock (LFRQ-N) level 4 internal interrupts have the same priority level as the Processor level 4 interrupt (second priority).
When the Bus Controller senses one of these inputs, the Bus Controller informs the CPU of an interrupt with NEXT-N and the CPU responds with SCM3-N as discussed previously for the Processor system interrupts. If no other DDT's or interrupts are being requested, the Bus Controller generates SACK-N (no request-select lines are involved). As discussed for the level 4 through level 1 interrupts, the Bus Controller generates HOLD-N and a binary code (ILOR-N and ILlP-N which represents the Interrupt level) that are routed to the CPU. The Bus Controller then generates data lines DBOO-N through DB02-N which is a 3-bit device number. A different device number is generated for each of the three internal interrupts. As a result the CPU is able to distinguish between the three level 4 internal interrupts and the level 1 self-interrupt.

5-50. The Bus Controller then generates STRB-N and DNOL-P and removes SACK-N. The CPU reads the device number generated by the Bus Controller and then generates DONE-N to indicate a completion. The Bus Controller then removes STRB-N which frees the INFIBUS. The CPU, under controller of the stored software program, jumps tc a subroutine to handle the internal interrupt

5-51. The Bus Controller generates CLKA--N which is a 25 MHz square wave used by the Autoload, Modem Controller 1, Block Transfer Adapter, Mag Tape Controller, I/O Controller, Modem Controller 2, and Program Maintenance Panel functions for timing purposes.

5-52. REPB-N is generated by the Program Maintenance Panel and routed to the Bus Controller whenever the reset switch located on the front panel is depressed. REPB-N causes the Bus Controller to generate MRCS-N (master reset) which clears all Processor functions with the exception the CPU.

5-53. CPU. The central processor unit (CPU) executes the software program stored in the Core Memory and processes data that is stored in the Core Memory or received from other Processor functions. It also routes data to or from other Processor functions and Core Memory, formats data, and under the control of the stored software program controls the operation of the Processor. The CPU operates as a master or a slave and performs internal arithmetic and logical operations independent of other Processor functions which minimizes its utilization of the INFIBUS.

5-54. The CPU is connected to the Bus Controller through the interconnecting module for the handling of Interrupts. While handling interrupts the CPU performs automatic save and restore of the program count and status. The interrupting device number is also) saved prior to the CPU's **automatic** jump to the prestored interrupt vector location of the interrupting level in the Core Memory.

5-55. When the CPU requires the INFIBUS for a data transfer it generates a CPU interrupt (SELC-N is generated) as explained previously. The CPU also operates as a slave and recognizes its internal register addresses when they are on the INFIBUS. Data can be either written into or read out of these registers (depending on the level of RITE-N) by either master Processor functions.

5-56. CORE MEMORY CONTROLLER. The Core Memory Controller is a slave which interfaces the Core Memory with the INFIBUS. It transfers assigned Core Memory addresses to the Core Memory and transfers data to or from the Core Memory. Commands from the INFIBUS are coupled through the Core Memory Controller to the Core Memory to perform read or write operations of words (16-bits) or bytes (8-bits) in assigned

addresses. The Core Memory Controller can only be slaved by other master Processor functions and cannot request access to the INFIBUS.

5-57. The Core Memory Controller is assigned addresses 0000 1_6 through EFFF 1_6 for storing the system software program and data. Address 0000 1_6 through 00FF 1_6 are known as the executive space of the Core Memory. Whenever an address from 0000 1_6 through BFFF 16 is detected on the INFIBUS by the Core Memory Controller, and a read or write operation is performed at the selected Core Memory Address, Addresses C000 $_{16}$ through DFFF 1_6 are used to transfer data in or out of areas in the Core Memory referred to as pages. There are 16 pages that may be assigned for use in the Core Memory (only two used) and the same address range is used for all 16 pages. To determine which page data is to be transferred to or from the Core Memory Controller must be first set at the particular page number. Whenever a page address is sensed on the INFIBUS by the Core Memory Controller, the Core Memory Address is shifted to the right (divided by two) by dropping the least significant bit and the page number (0 or 1) is inserted in the most significant bit.

5-58. To read or write into a page of Core Memory, the master first places FFFF 16 on the INFIBUS address lines and the selected page number, 0000 1_6 through 000F l6, on the data lines with the RITE-N line low for a write operation. The Core Memory Controller senses this and the page number is written into in an Internal register when STRB-B is generated by the master. Now when the page addresses are used they will be modified by having the most significant four bits replaced with the stored page number and then presented to the Core Memory to transfer data into or out of the page. To transfer data out of or into another page, the cycle of selecting the page must be repeated to set the Core Memory Controller internal register. To determine which page the Core Memory Controller has been previously set at, the Internal register is addressed, FFFF 16, with a read operation requested (RITE-N high) and the page number is presented on the INFIBUS data lines to be read by the requesting function.

5-59. AUTOLOAD. The Autoload function is a masterthat contains a fixed, stored instruction set (ROM program) which is used to control loading of the operating program or utility print program (UPP) in the Core Memory. The Autoload function can perform direct data transfers on the INFIBUS and can also generate a level 1 interrupt request for INFIBUS access.

5-60. The Autoload function is initiated when the INFIBUS Autoload, ATLD-N, line is activated. ATLD-N is generated by the Bus Controller after power turn on; if enabled as discussed previously or by the operator pressing the lighted load switch on the front panel. When the operator presses the reset switch on the front panel, the Program Maintenance Panel generates REPB-N which causes the Bus Controller to generate master reset, MRES-N. MRES-N clears all Processor functions and causes the load switch located on the front panel to light. The operator must load a program tape on a Mag Tape Unit and then with the lighted load switch depressed the Program Maintenance Panel generates ATLD-N which is sensed by the Autoload function.

5-61. The Autoload function, after sensing ATLD-N, performs a DDT as explained previously. During this DDT, the address 0005 16 is placed on the address lines, AB00-N through AB15-N, the Autoload address, FB00 16, is placed on the data lines, DB00-N through DB15-N, and RITE-N is generated. This causes the Autoload address to be stored in the Core Memory. The Core Memory Controller then indicates the data is stored in the Core Memory by generating DONE-N which causes the Autoload to free the INFIBUS by removing STRB-N.

5-62. After the DDT, the Autoload function initiates a level 1 interrupt by generating SRLl-N. The level 1 interrupt IS performed as explained previously. The CPU then grants the Autoload function INFIBUS access by placing the Autoload address (stored in Core Memory during DDT) on the address

lines. When the Autoload senses its address on the INFIBUS lines, the first ROM data word is placed on the data lines. The CPU reads this data then addresses the Autoload function again and increases the Autoload address by two to FB02 1_6. This occurs eight times and each time a new ROM data word is read by the CPU and placed in the Core Memory. The CPU then uses these eight data words to initialize the Mag Tape Controller and Block Transfer Adapter. The Mag Tape Controller and Block Transfer Adapter then load the operating program or utility print program into a buffer area in the Core Memory. When the entire program is loaded into the buffer area, the Autoload function is again addressed and the Autoload ROM program is read by the CPU. The program stored in the buffer area of the Core Memory is then transferred to the proper location in Core Memory. The last data word of the program will cause the Processor to either halt or execute the last instruction of the program which may cause the CPU to jump to the beginning of the operating program.

5-63. PARALLEL I/O. The Parallel I/O function receives 12-bit words of data from the INFIBUS and couples These data bytes and control signals to the Alarm Control and VF Comm Link function. It also receives 12-bit data words and control signals from the Alarm Control and VF Comm Link function and couples these data bytes to the INFIBUS. The Parallel I/O receives data under control of the stored software program that controls various lamps on the Alarm Panel. It also receives various alarm conditions from the Alarm Control and VF Comm Link function. These alarms are used to notify the Processor of external failures such as blown fuses, mag tape not ready and executive program alarm. The Parallel I/O also enables the Alarm Control and VF Comm Link function, under stored software program control, to output a phone number, and, when the call is answered cuts the VF Comm Link 1 function into the communications link. In the ACOC group, the Parallel I/O can cut either the VF Comm Link 1 or VI' Comm Link 2 into the communications link.

5-64. The Parallel I/O function is a slave that generates a level 1 interrupt and is assigned address F92X 16. There are three registers located in the Parallel I/O; the data register, control register, and status register. Each register is assigned a separate address which allows the stored software program to write into or read from each register as determined by the level of RITE-N. The data register is assigned address F928 16. The control register address is F926 16, and the **Status** register is F920 16.

5-65. If the stored software program is to clear the Parallel I/O, F920 16 is placed on the INFIBUS address lines, AB00-N through AB15-N. Also, no data is placed on the INFIBUS data lines, DB00-N through DB15-N, and a write operation (RITE-N low) is performed. This write operation to the status register clears the Parallel I/O. The Parallel I/O then generates DONE-N which frees the INFIBUS.

5-66. The stored software program can also read from or write into the control register, as determined by the level of RITE-N, by placing the control register address on the INFIBUS address lines. After the control register is written into or read from, the Parallel I/O generates DONE-N which frees the INFIBUS.

5-67. Under control of the CPU, the Parallel I/O is enabled to generate or prevented from generating a level 1 interrupt whenever data is to be transferred by the Parallel I/O. The control word that has been loaded into the control register enables or disables the Parallel I/O INFIBUS access circuits which generate the level 1 interrupt. If the level 1 interrupt is disabled by the control word, the CPU regularly checks status (reads status register) to determine whether a data transfer is to be performed. When the Alarm Control and VF Comm Link function notifies the Parallel I/O that data is to be transferred, a programmed data transfer (PDT) status bit is set in the status register. When the CPU detects the PDT status bit, the CPU jumps to a subroutine which determines whether a write or read operation is to be performed. If a write operation is to be performed by the CPU, the CPU places the data register address on the INFIBUS address lines, places the data on the

INFIBUS data lines, and generates RITE-N. The data is loaded into the Parallel I/O which then generates DONE-N to free the INFIBUS. The Parallel I/O now clocks the input data from the INFIBUS to the Alarm Control and VF Comm Link 1 function. If a read operation is to be performed by the CPU, the CPU places only **the data register** address on the INFIBUS address lines and the parallel data from the Alarm Control and VF Comm Link 1 function which is now loaded into the Parallel I/O is strobed to the INFIBUS data lines. The Parallel I/O then generates DONE-N to free the INFIBUS.

5-68. If the level 1 Interrupt IS enabled by the control word in the control register, whenever the PDT **status** bit is set, a level 1 interrupt IS generated, as explained previously. The CPU then addresses the data register and performs a read or write operation in the same manner as when the level 1 Interrupt was disabled.

5-69. TTY CONTROLLER. The TTY Controller function receives **8-bit bytes** of data from the INFIBUS and converts **these bytes to** 11-bit, ASCII coded, serial words that are **routed to the** TTY function. It also receives: 11-bit, ASCII coded, serial words from the TTY function and converts these words to 8-bit bytes of data that are placed or the INFIBUS. The TTY Controller is a slave that generates a level 2 interrupt and is assigned address F8OX 16. There are three registers located in the TTY Controller; the data register, control register, and status register. Each register is assigned a separate address which allows the stored software program to write into or read from each register as determined by the level of RITE-n;. The data register is assigned address F808 16. The control register address is F806 16 and the status register is F800 16.

5-70. If the stored software program is to clear the TTY Controller, $F800_{16}$ is placed on the INFIBUS address lines, AB00-N through AB15-N and no data is placed on the INFIBUS data lines, DB00-N through DB15-N, and a write operation (RITE-N low) is performed. This write operation of the status register clears the TTY Controller. The TTY Controller then generates DONE-N which frees the INFIBUS.

5-71. The stored software program can also read from or write into the control register, as determined by the level of RITE-N.. by placing the control register address on the INFIBUS address lines. After the control register is written into or **read** from, the TTY Controller generates DONE-N which frees the INFIBUS.

5-72. Under control of the CPU, the TTY Controller is enabled to generate or prevented from generating a level 2 interrupt whenever data is to be transferred by the TTY Controller. The control word that has been loaded into the control register enables or disables the TTY Controller INFIBUS access circuits which generate the level 2 Interrupt. If the level 2 interrupt is disabled by the control word, the CPU regularly checks status (reads status register) to determine whether a data transfer is to be performed. When the TTY function notifies the TTY Controller that data is to be transferred, a programmed data transfer (PDT) status bit is set in the status register. When the CPU detects the PDT status bit, the CPU lumps to a subroutine which determines whether a write or read operation is to be performed. If a write operation is to be performed by the CPU, the CPU places the data register address on the INFIBUS address lines, places the data on the INFIBUS data lines, and generates RITE-N. The data is loaded into the\TTY Controller which then generates DONE-N to free the INFIBUS. The TTY Controller now converts the parallel input data from the INFIBUS to serial data that is clocked to the TTY function. If a read operation is to be performed, the CPU places only the data register address on the INFIBUS address lines and the serial data from the TTY function which has been converted to an 8-bit parallel byte is strobed to the INFIBUS data lines. Then the TTY Controller generates DONE-N to free the INFIBUS.

5-73. If the level 2 interrupt IS enabled by the **control** word in the control register, whenever the PDT status bit is set, a level 2 interrupt is generated, as explained pre-

viously. The CPU then addresses the data register and performs a read or write operation in the same manner as when the level 2 interrupt was disabled.

5-74. The baud rate of the TTY Controller is controlled by a signal from the TTY function which is derived from the line frequency Therefore, if the line frequency varies which in turn varies the speed of the TTY motor, the baud rate varies proportionately.

5-75. MODEM CONTROLLER 1. The Modem Controller 1 function receives 8-bit bytes of data from the INFIBUS and converts these bytes to serial words that are routed to the VF Comm Link 1 function. It also receives serial words from the VF Comm Link 1 function and converts the words to 8-bit bytes of data that are placed on the INFIBUS. Modem Controller 1 is a slave that generates a level 2 interrupt and is assigned address F93X 16. There are three registers located in Modem Controller 1; the data register, control register, and **status** register. Each register is assigned a separate address which allows the stored software program to write into or read from each register as determined by the level of RITE-N. The data register is assigned address F938 16. The control register address is F936 16, and the status register is F930 16.

5-76. If the stored software program is to clear Modem Controller 1, F930 16 is placed on the INFIBUS address lines, ABOO-N through AB15-N and no data is placed on the INFIBUS data lines, DBOO-N through DB15-N, and a write operation (RITE-N low) is performed. This write operation to the status register clears Modem Controller 1. Modem Controller 1 then generates DONE-N which frees the INFIBUS.

5-77. The stored software program can also read from or write into the control register, as determined by the level of RITE-N, by placing the control register address on the INFIBUS address lines. After the control register is written into or read from, Modem Controller 1 generates DONE-N which frees the INFIBUS.

5-78. Under control of the CPU, Modem Controller 1 is enabled to generate or prevented from generating a level 2 interrupt whenever data is to be transferred by Modem Controller 1. The control word that has been loaded into the control register enables or disables Modem Controller 1 INFIBUS access circuits which generate the level 2 interrupt. If the level 2 interrupt is disabled by the control word, the CPU regularly checks status (reads status register) to determine whether a data transfer is to be performed. When the VF Comm Link 1 function notifies Modem Controller 1 that data is to be transferred, a programmed data transfer (PDT) status bit is set in the status register. When the CPU detects the PDT status bit, the CPU jumps to a subroutine which determines whether a write or read operation is to be performed,. If a write operation is to be performed by the CPU, the CPU places the data register address on the INFIBUS address lines, places the data on the INFIBUS data lines, and generates RITE-N. The data is loaded into the Modem Controller 1 which then generates DONE-N to free the INFIBUS. Modem Controller 1 now converts the parallel input data from the INFIBUS to serial data that is clocked to the VF Comm Link 1 function. If a read operation is to be performed, the CPU places only the data register address on the INFIBUS address lines and the serial data from the VF Comm Link 1 function which has been converted to an 8-bit parallel byte is strobed to the INFIBUS data lines. The Modem Controller 1 then generates DONE-N to free the INFIBUS.

5-79. If the level 2 interrupt is enabled by the control word in the control register, whenever the PDT status bit is set, a level 2 interrupt is generated, as explained previously. The CPU then addresses the data register and performs a read or write operation in the same manner as when the level 2 interrupt was disabled.

5-80. Modem Controller 1 operates at 1200 baud which is derived from the clock signal, CLKA-N, from the INFIBUS.

5-81. BLOCK TRANSFER ADAPTER. The Block Transfer Adapter is a master which

enables the Mag Tape Controller to transfer a group of data bytes (called blocks) = These blocks are transferred directly to the Core Memory during the loading of an operating program, to or from the RMR function during rapid memory reload, or to the TTY function after the utility print program has been loaded.

5-82. To transfer a block of data from the Formatter function, the Formatter causes the Mag Tape Controller to generate a level 3 interrupt. To transfer a block of data to the Formatter function the stored software program determines when data is to be transferred. In both of these cases, the Mag Tape Controller and Block Transfer Adapter status registers (address F8C0 16) are written into which clears both functions. When both functions are cleared the Mag Tape Controller generates DONE-N which frees the INFIBUS. Then the CPU addresses the Mag Tape Controller and Block Transfer Adapter control registers (address F8C6 16) and loads a control word from the INFIBUS data lines, DB00-N through DB15-N, into the control registers. This control word idles the Block Transfer Adapter and enables the Mag Tape Controller to transfer data. The CPU new initializes the Mag Tape Unit via the Mag Tape Controller and Formatter functions. The CPU then generates a second control word that idles the Mag Tape Controller and enables the Block Transfer Adapter. The CPU now writes the block length (number of blocks to be transferred) into the Block Transfer Adapter block length register (address F8C4 16). When the block length is loaded in the block length register the Block Transfer Adapter generates DONE-N which frees the INFIBUS. The CPU then loads one of the following addresses into the Block Transfer Adapter address register (address F8C2 16): start address (if the data is to be read from or written into Core Memory), RMR address (if the data is to be read from or written into the RMR function), or the TTY function address (utility print program).

5-83. The CPU now loads a control word into the Block Transfer Adapter and Mag Tape Controller control register that enables the Mag Tape Controller and Block Transfer Adapter to perform read (to INFIBUS) or write (from INFIBUS) operations. When the Mag Tape Controller is ready to begin transfers, it notifies the Block Transfer Adapter via the BTA control lines, BTA1-N through BTA4-N. This control word also causes the Block Transfer Adapter to operate as a master.

5-84. The Block Transfer Adapter now generates a DDT, as explained previously, which places the starting address on the INFIBUS address lines, AB00-N through AB15-N. If a write operation is to be performed RITE-N is generated and the data from the INFIBUS data lines is loaded into the Mag Tape Controller. When the Mag Tape Controller accepts the data, it generates DONE-N which frees the INFIBUS. This data is clocked through the Mag Tape Controller to the Formatter. At the same time, the Block Transfer Adapter block length register is decremented by one and the address register is incremented by one. After the data is clocked through the Mag Tape Controller, it notifies the Block Transfer Adapter, via the BTA control lines, that it is ready to perform another transfer and the sequence is repeated (except address is increased by one) until the block length register is at zero.

5-85. If a read operation is to be performed, RITE-N is not generated and the Mag Tape Controller places the data on the INFIBUS data lines. The Mag Tape Controller then generates DONE-N which frees the INFIBUS. At the same time the block length register decrements by one and the address register increments by one. The Mag Tape Controller notifies the Block Transfer Adapter that it is ready to perform another data transfer and the sequence is repeated (except address is increased by one) until the block length register is at zero.

5-86. When the block length register reaches zero, all Mag Tape Controller and Block Transfer Adapter operations cease. Also, the Mag Tape Controller generates a level 3 interrupt which notifies the CPU that the block transfer is complete. The CPU then reinitializes the Mag Tape Controller and Block Transfer Adapter with a new block length and, starting address. This

sequence is continued until al1 blocks of data are transferred.

5-87. When the Block Transfer Adapter and Mag Tape Controller are used to print out message tapes under control of the utility print program, the address register is loaded with the TTY function address and it is not decremented after the data is written out.

5-88. MAG TAPE CONTROLLER. The Mag Tape Controller function transfers bytes of data between the Formatter function and INFIBUS. When not under control of the Block Transfer Adapter, the Mag Tape Controller transfers data to and from the For - matter and INFIBUS, under control of the stored software progrom. This data is used to initialize the Formatter and notify the CPU of the Formatter status.

5-89. I/O CONTROLLER. The I/O Controller function is a master which controls data transfers between the CCL, RSJ, or RMR functions and the INFIBUS. It can also be addressed (slaved) by the stored software program via the CPU. The I/O Controller also determines which function has priority when more than one function is requesting the INFIBUS.

5-90. When the CCL or RSJ function is requesting a direct memory access (DMA), the i/O Controller generages a DDT and strobes the address, data and control information from the function. requesting the DMA to the INFIBUS.

5-91. When the CCL, RSJ, or RMR function generates an interrupt request, the I/O Controller generates a level 2 interrupt as explained previously and strobes the device number of the function requesting the interrupt to the INFIBUS data lines.

5-92. The I/O Controller is assigned address F88X 16. When, address F880 16 is on the INFIBUS address lines, ABOO-N through AB15-N, the RSJ function is enabled to perform a read or write operation. The CCL function is enabled when F882 16 is on the INFIBUS address lines. The RMR function is enabled when F884 is on the INFIBUS address lines. To notify the RMR function of a CPU data request, F88B is placed on the INFIBUS address lines. When F886 16 is on the INFIBUS address lines and RITL-N is low, the data command word from; the stored software program on the INFIBUS data lines, DBOO-N through DB15-N, is strobed into the I/O Controller to select the desired mode of operation of the CCL, RSJ, or RMR functions.

5-93. PRINTER CONTROLLER (ACOC Group Only). The Printer Controller function receives 8-bit bytes of data from the INFIBUS and converts these bytes to 11-bit, ASCII coded, serial words that are routed to the RO TTY function. It also receives 11-bit, ASCII coded, serial words from the RO TTY function and converts these words to 8-bit bytes of data that are placed on the INFIBUS. The Printer Controller is a slave that generates a level 2 interrupt and is assigned address F81X 16. There are three registers located in the Printer Controller; the data register, control register, and status register. Each register IS assigned a separate address which allows the stored software program to write into or read from each: I register as determined by the level of RITE-N. The data register is assigned address F818 16. The control register address is F816 16, and the status register is F810 16.

5-94. If the stored software program: is to clear the Printer Controller, F810 16 is placed on the INFIBUS address lines ABOO-N through AB15-N and no data is placed on the INFIBUS data lines, DB00-N through DB15-N, 2nd a write operation (RITE-N low) IS performed. This write operattion to the status register clears the Printer Controller. The Prlntcr Controller then generates DONE-N which frees the INFIBUS.

5-95. The stored software program can: also read from or write into the control register, as determined by the level of RITE-N by placing the control register address on the INFIBUS address lines. After the control register is written into or read from the Printer Controller generates DONE-N which frees the INFIBUS.

5-96. Under control of the CPU, the Printer Controller is enabled to generate or prevented from generating a level 2 interrupt--whenever data is to be transferred by the Printer Controller. The control word that has been loaded into the control register enables or disables the Printer Controller INFIBUS access circuits which generate the level 2 interrupt. If the level 2 interrupt is disabled by the control word, the CPU regularly checks status (reads status register) to determine whether a data transfer is to be performed. When The RO TTY function notifies the Printer Controller that data is to be transferred a programmed data transfer (PDT) status bit is set in the status register. When the CPU detects the PDT status bit, the CPU jumps to a subroutine Which determines whether a write or read operation IS to be performed. If a write operation is to be performed by the CPU, the CPU places the data register address on the INFIBUS address lines, places the data on the INFIBUS data lines, and generates RITE-N. The data is loaded into the Printer Controller which then generates DONE-N to free the INFIBUS. The Printer Controller now converts the parallel input data from the INFIBUS to serial data that IS clocked to the RO TTY function. If a read operation is to be performed, the CPU places only the data register address on the INFIBUS address lines and the serial data from the RO TTY function which has been converted to an 8-bit parallel byte is strobed to the INFIBUS data lines. The Printer Controller then generates DONE-N to free the INFIBUS.

5-97. If the level 2 interrupt is enabled by the control word in the control register, whenever the PDT status bit is set, a level 2 interrupt is generated, as explained previously. The CPU then addresses the data register and performs a read or write operation in the same manner as when the level 2 Interrupt was disabled.

5-98. The baud rate of the Printer Controller is controlled by a signal from the RO TTY function which is derived from the line frequency. Therefore, if the line frequency varies which in turn varies the speed of the RO TTY motor, the baud rate varies proportionately.

5-99. MODEM CONTROLLER 2 (ACOC Group only). The Modem Controller 2 function receives S-bit bytes of data from the INFIBUS and converts these bytes to serial words that are routed to the VF Comm Link 2 function. It also receives serial words from the VF Comm Link 2 function and converts these words to 8-bit bytes of data that are placed on the INFIBUS. Modem Controller 2 is a slave that generates a level 2 interrupt and is assigned address F94X 16. There are three registers located in Modem Controller 2; the data register, control register, and status register. Each register is assigned a separate address which allows the stored software program to write into or read from each register as determined by the level of RITE-N. The data register is assigned address F948 16. The control register address is F946 16, and the status register is F940 16.

5-100. If the stored software program is to clear Modem Controller 2, F940 16 is plated on the INFIBUS address lines, ABOO-N through AB15-N, no data is placed on the INFIBUS data lines, DBOO-N through DB15-N, and a write operation (RITE-N low) is performed. This write operation to the status register clears Modem Controller 2. Modem Controller 2 then generates DONE-N which frees the INFIBUS.

5-101. The stored software program can also read from or write into the control register, as determined by the level of RITE-N, by placing the control register address on the INFIBUS address lines. After the control register is written into or read from, Modem Controller 2 operates DONE-N which frees the INFIBUS.

5-102. Under control of the CPU, Modem Controller 2 is enabled to generate or prevented from generating a level 2 interrupt whenever data is to be transferred by Modem Controller 2. The control word that has been loaded into the control register enables or disables Modern Controller 2 INFIBUS access circuits which generate the level 2 interrupt. If the level 2 interrupt is disabled by the control word, the CPU regularly checks status (reads status register) to determine whether a data transfer is to be performed. When the VF Comm Link 2

function notifies Modem Controller 2 that data is to be transferred, a programmed data transfer (PDT) status bit is set in the status register. When the CPU detects the PDT status bit, the CPU jumps to a subroutine which determines whether a write or read operation is to be performed. If a write operation is to be performed by the CPU, the CPU places the data register address on the INFIBUS address lines, places the data on the INFIBUS data lines, and generates RITE-N. The data is loaded into Modem Controller 2 which then generates DONE-N to free the INFIBUS. Mode:., Controller 2 now converts the parallel input data from the INFIBUS to serial data that is clocked to the VF Comm Link 2 function. If a read operation is to be performed, the CPU places only the data register address on the INFIBUS address lines and the serial data from the VF Comm Link 2 function which has been converted to an 8-bit parallel byte is strobed to the INFIBUS data lines. The Modem Controller 2 then generates DONE-N to free the INFIBUS.

5-103. If the level 2 interrupt is enabled by the control word in the control register, whenever the PDT status bit is set, a level 2 interrupt is generated, as explained previously. The CPU then addresses the data register and performs a read or write operation in the same manner as when the level 2 interrupt was disabled.

5-104. Modem Controller 2 operates at 1200 baud which is derived from the clock signal, CLKA-N, from the INFIBUS.

5-105. PROGRAM MAINTENANCE PANEL. The Program Maintenance Panel function enables an operator to manually enter address, data, and control inputs to the Processor. It allows the operator to read from or write into (DDT) any addressable area of the Processor and usually operates as a master. It can also, under control of the stored software program, display on the front panel various steps within the program (operates as a slave). The Program Maintenance Panel also generates a level 1 interrupt when the attention (attn) switch located on the front panel is depressed.

5-106. CORE MEMORY FUNCTIONAL BLOCK DIAGRAM DESCRIPTION.

5-107. GENERAL. The following paragraphs contain a functional block diagram discussion of the Core Memory (figure 5). The Switch Group Core Memory contains 8 Core Memory Basic Storage Modules (CM BSM) and the ACOC Core Memory contains 8. CM BSM's, therefore, this discussion will discuss a system with one CM BSM, unless applicable.

5-108. The Core Memory can operate in four modes: clear/write, read/restore, read/modify/write, and read only. However, only the clear/write and read/restore modes are functional. The read/modify/write mode is not functional because FULL CYC-P is always 5 volts. The read only mode is not functional because RD ONLY-P is always 0 volts. In the clear/write mode all of the cores at the selected address are cleared (returned to logic 0) and any data generated is not read out of the Core Memory. in the read-restore mode the data is read out of the selected address and the same data is returned to that address. In the read/modify/write mode the data is read out of the selected address and new or revised data is placed into that address of the Core Memory. In the read only mode the data is read out of the selected address and that address is left cleared. The read only mode is not functional in the Core Memory because RD ONLY-P is tied to logic 0 in the Processor Core Memory Controller. The clear/write and read/restore modes are known as full cycle modes, The read/modify/write mode is known as a split cycle because of the tlming pause before instructions are received by the Core Memory to per form the write operation. Each of the two functional modes may use either synchronous or a asynchronous cycle reinitiate.

5-109. With synchronous cycle reinitiate, signal RD INIT-P or WT INIT-P from the Processor Core Memory Controller to the CM MIA timing and control logic circuits is returned to logic 0 before the end of the cycle. To initiate the next cycle, RD: INIT-P or WT INIT-P goes to logic 1.

5-110. With asynchronous cycle reinitiate, the control signals may assume their appropriate values prior to the end of a cycle in progress. The next cycle is then automatically initiated by the Core Memory when MEM AVAIL-P returns to logic 1.

5-111. In the clear/write mode zone control signals, ZW1-P and ZW2-P, cause byte operation of the Core Memory. In the clear/write mode, if both ZW1-P and ZW2-P are logic 1, clear/write mode is performed on the word. In the clear/write mode, if ZWl-P is logic 1 and ZW2-P is logic 0, a clear/write operation is performed on byte 1 (DI00-P through DI08-P) and 1 read/restore operation is performed on byte 2 (DI09-P through DI17-P). In the clear/write mode, if ZWl-P is logic 0 and ZW2-P is logic 1, a read/restore operation is performed on byte 1 and a clear/write operation is performed on byte 2.

5-112. The two functional modes of the Core Memory are described in the following paragraphs.

5-113. CLEAR/WRITE MODE. The clear/write mode is used to store data into the core memory stack without referece to the data already stored in the selected address. The core memory stack location is first cleared then the new data is written in. The clear portion is a read cycle but the data is not read out. The cycle initiated by the Processor Core Memory Controller signal WT INIT-P going to logic 1 with the following conditions; RD INIT-P at logic 0, RD ONLY-P at logic 0, and FULL CYC-P at logic 1. Under these conditions, AIX-P is generated which clocks address bits AI00-P through AI15-P from the Processor Core Memory Controller into the address registers 00 through 15. The outputs of address registers 00 through 12, MAR00-P through MAR12-P, are applied to the address decoding and switching circuits. Address bits AI13-P, AI14-P, and AI15-P are decoded by the address registers 13, 14, and 15. The outputs of the address registers 13, 14, and 15, BSM00-P through BSM03-P, enable the selected CM BSM. 50 nsec after AIX-P is generated MEM AVAIL-P goes low to notify the Processor Core Memory Controller that the Core Memory is busy. RDR-P is now generated which clears the data register. The timing and control logic circuits now generate PRE YRT-P and MRT-P which cause the control and buffer logic circuits to generate XRTl-P, XRT2-N, and YRT-N. This causes the address decoding and switching circuits and X and Y current sources to generate the appropriate X read currents, XCA0-P through XCA7-P and XSOO-P through XS15-P, and Y read currents, YCAO-P through YCA7-P and YS00-N through YS07-N, as determined by MAR00-P through MAR12-P. The X read currents cause current flow through one of the 128 X lines from the X diode matrix and the Y read currents cause current flow through one of the 64 Y lines from the Y diode matrix. At the cores where these lines intersect, if a one was stored, core turnover occurs. Where a core turnover occurs a pulse is coupled to the appropriate sense line, S-00 through S-17, however, because the sense amplifiers are not enabled by SAS-P this data is not strobed through the sense amplifiers. This clears the selected address within the core memory stack. The write portion of the cycle begins as the Processor Core Memory Controller data input signals, DI00-P through DI17-P, are clocked into the data register by timing and control logic signal DIX-P; Data inhibit signals DATA INH00-P through DATA INH17-P, from the data register are strobed through the inhibit drivers by TINH-P. The inhibit drivers generate the inhibit signals, INH00-N through INH17-N, wherever a logic 0 is to be stored in the core memory stack. Controlled by timing and control logic signal MWT-P, control and buffer logic circuit generates signals WT1-P and WT2-P. This causes the address decoding and switching circuits and X and Y current sources to generate the appropriate X write currents, XCC0-N through XCC7-N and XS00-P and XS15-P, and Y write currents, YCC0-N through YCC7-N and YS00-P and YS07-P, a:; detcrmined by MAR00-P through MAR12-P. When the data is written into the selected address, MEM AVAIL-P returns to logic 1 indicating to the Processor Core Memory Controller that a new cycle may be initiated.

5-114. READ/RESTORE MODE. The read/restore mode reads information from the core memory stack address and then returns the same information to the same location in the core memory stack. The read portion of the cycle is initiated by the Processor Core Memory Controller output signal RD INIT-P going to logic 1 with the following conditions: WT INIT-P at logic 0, RD ONLY-P at logic 0, and FULL CYC-P at logic 1. Under these conditions, timing and control logic signal AIX-P clocks address bits AIOO-P through AI15-P into the address registers. The outputs of address registers 00 through 12, MAROO-P through MAR12-P, are applied to the address decoding and switching circuits. Address bits AI13-P, AI14-P, and AI15-P are decoded by the address registers 13, 14, and 15. The outputs of the address registers 13, 14, and 15, BSMOO-P through BSMO3-P, enable the selected CM BSM. 50 nsec after AIX-P is generated MEM AVAIL-P goes low to notify the Processor Core Memory Controller that the Core Memory is busy. RDR-P is now generated which clears the data register. The timing and control logic circuits now generate PRE YRT-P and MRT-P which cause the control and buffer logic circuits to generate XRTl-P, XRT2-N, and YRT-N. This causes the address decoding and switching circuits and X and Y current sources to generate the appropriate X read currents, XCAO-P through XCA7-P and XSOO-P through XS15-P, and Y read currents, YCAO-P through YCA7-P and YSOO-N through YS07-N, as determined by MAROO-P through MAR12-P. The X read currents cause current flow through one of the 128 X lines from the X diode matrix and the Y read currents cause current flow through one of the 64 Y lines from the Y diode matrix. At the cores where these lines intersect, if a one was stored, core turnover occurs. Where a core turnover occurs a pulse is coupled to the appropriate sense line, S-00 through S-17.

5-115. MSAS-P enables the data register to receive the output data, causes the control and buffer logic circuits to generate SAS-P, and causes the data register to generate SASl-P and SAS2-P. Output signals S-00 through S-17 from the core memory stack are coupled through the sense amplifiers which are enabled by SAS-P. The sense amplifiers outputs, SAOO-P through SA17-P are coupled through the sense gates which are enabled by SAS1 -P and SAS2-P. The sense gates outputs, MDROO-P through MDR17-P, are loaded into the data register by TDOX-P. DATA AVAIL-N now goes to logic 0 indicating that the requested information is available. Signals MDROO-P through MDR17-P now determine the level of DATA INHOO-P through DATA INH17-P. The restore portion of the cycle is initiated when timing and control logic signal TINH-P is sent to the inhibit drivers, resulting in the generation of inhibit current signals INHOO-N through INH17-N through the cores in the core memory stack where a logic 0 is to be restored. Write timing signals WTl-P and WT2-P are ‘now sent to the address decoding circuitry, resulting in the generation of X and Y write currents, as explained previously. Timing and control logic signal ME M AVAIL-P returns to logic 1 indicating that a new cycle may be initiated.

5-116. PROCESSOR DETAIL LOGIC DIAGRAM DESCRIPTION.

5-117. GENERAL. The following paragraphs contain the detail logic diagram discussions for the Processor functions. The Bus Controller function consists of the service request selection and interrupt circuits and alarm and INFIBUS timing circuits. The CPU consists of the sequence register and control storage circuit, microcode register circuit, control circuit, receive register circuit, transmit register circuit, address register circuit, arithmetic logic unit (ALU) input multiplexer circuit, ALU circuit, register file circuit, carry and overflow circuit, emulation instruction register circuit. address recognition circuit, INFIBUS access circuit, and central timing circuit. The Core Memory Controller consists of the command and page select circuit, address transfer circuit, and data transfer circuit. The Autoload function consists of the control circuit, address recognition and ROM select circuit, INFIBUS access circuit, and ROM and data circuit. The Parallel I/O function consists of the address recognition

circuit, INFIBUS access circuit, data input and selector circuit, data output and control register circuit, and read/write control status circuit. The TTY Controller, Modem Controller 1, Printer Controller, and Modem Controller 2 functions operate in a similar manner. Therefore, the discussions supporting these functions have been combined under the Serial I/O control group heading. The Serial I/O control group functions consist of the address recognition circuit, INFIBUS access circuit, clock generator circuit, control register circuit, data selector control circuit, and asynchronous data transfer control circuit. The Mag Tape Controller function consists of the address recognition circuit, INFIBUS access circuit, data input and selector circuit, data output and control register circuit, and read/write control status circuit. The I/O Controller function consists of the clock circuit, address recognition, done and reset circuit, data circuit, interface circuit, and INFIBUS access circuit. The Program Maintenance Panel function consists of the address/data switch identification, multiplexers, and LED circuit, CPU register selection circuit, address multiplexer, bus driver receiver, and recognition circuit, data multiplexer and bus driver receiver circuit, switch flip-flops and single action discriminator circuit, miscellaneous control circuit, state generation and micro-operations circuit, and INFIBUS access circuit.

5-118. BUS CONTROLLER A1A3A5 SERVICE REQUEST SELECTION AND INTERRUPT CIRCUIT.

5-119. General. The Bus Controller service request selection and interrupt circuit allocates INFIBUS time to Processor functions for information transfers on a priority basis. It receives and services two direct data transfer (DDT) requests a and four **levels** of Interrupt requests. The lowest priority is the DDT request used by the CPU to transfer the stored software programs and data. The highest priority is the DDT request used by Processor masters to transfer data direct**ly** to and from Processor functions. In between are the level 1 through 4 Interrupts, lowest priority to highest, used by Processor functions to transfer data under CPU control.

5-120. Detail Analysis (see figure 6). After power is applied to the Processor, RSET-N is received from the Bus Controller alarm and INFIBUS timing circuit which clears flip-flop FF3 and mask flip-flops U71 (flip-flop FF2 shown typical). This enables gates Gl, G4, G6, G11, G13 and G16. RSET-N also activates gate G42 which generates SCRS-N which is routed to the Bus Controller alarm and INFIBUS timing circuit. SCRS-N also resets the interrupt level flip-flops U65 (flip-flop FF2 shown typical). The 1 output of FF3 (low) activates gates G19 and G43. The output of G19 disables gates G2, G5, G7, G12, G14 and G17. The output of G43, RNIR-P, is routed to the Bus Controller alarm and INFIBUS timing circuit. RNIR-P is also inverted by inverter I8, generating INAR-N which is routed to the Bus Controller alarm and INFIBUS timing circuit.

5-121. When a Processor master module is requesting a DDT, SRLD-N (highest priority) is generated on the INFIBUS. SRLD-N (waveform A, figure 7) is received by the Bus Controller service request selection and interrupt circuit and inverter I2 inverts SRLD-N activating gate G3. The output of G3 is routed to the 1D3 input of the 4-bit latch U43 and activates gate G9 which triggers 4-bit latches U43 and U52. The 4-bit latches U43 and US2 activate gate G10 which generates S11P-P (waveform B, figure 7). The 4-bit latch U43 also generates RLDS-P. Inverter 16 inverts RLDS-P which enables gate G22. The output of I6 also disables gates G23 and G25 and activates gate G26. The output of G26 disables gates G28, G30, G32, G36, and G38. At the same time, S11P-P enables gate G20 and delay DLl delays S11P-P by 20 nsec. After the 20 nsec delay, G20) is activated and its output is inverted by inverter I5 which activates gate G21. The output of G21 activates G22 which generates SELD-N (waveform C, figure 7). The **output** of G22 also activates gate G27 which generates

PCDI-P (waveform D, figure 7). PCDI-P generates the precedence pulse PCDA-P **Which is** routed to the INFIBUS.

5-122. The Processor master requesting the DDT receives SELD-N and the precedence pulse and then responds with SACK-N. The Bus Controller alarm and INFIBUS timing circuit' then generates RSAK-P (waveform E, figure 7) which is inverted by inverter I1. The output of I1, NSAK-N (waveform F, figure 7), is routed to the Bus Controller. alarm and INFIBUS timing circuit. NSAK-N also disables G3 and G21. G3 disables G9 and G21 disables G22 which causes SELD-N to return to high. The high output of G9 clears 4-bit latches U43 and U52, causing RLDS-P to return to low. The Processor master then removes SRLD-N and SACK-N. RSAK-P goes low and is inverted by I1 which enables G3 again. The Processor master selected transfers data on the INFIBUS and how another Processor master may request INFIBUS access but will not be serviced until the selected function completes the data transfer.

5-123. When a Processor function requests a level 4 interrupt, it generates SRL4-N . SRL4-N (waveform G, figure 7) from the INFIBUS activates G4 which enables G5 and activates gate G8. The output of G8 activates gate G18 which generates NEXT-N (waveform I-I, figure 7) which is routed to the CPU. When the CPU is ready to accept the interrupt, the CPU generates SCM3-N (waveform I, figure 7) which presets FF3 and activates G42. The 1 output of FF3 (high) disables G19 and G43. Disabled G19 enables G2, G7, G14, G12, G17 and activates G5. Disabled G43 causes RNIR-P (waveform Q, figure 7) to go low and I8 causes INAR-N (waveform R, figure 7) to go high. The output of G42, SCRS-N (waveform J, figure 7), is routed to the Bus Controller alarm and INFIBUS timing circuit. SCRS-N also clears the interrupt level flip-flops U65.

5-124. The output of G5 is applied to the 1Dl input of 4-bit latch U43 and activates G-3. The output of G9 triggers 4-bit latches U43 and U52 which causes the 05 output to go high and the O1 output of 4-bit latch U43 to go high, generating RL4S-P. The 05 outputs of 4-bit latch and U52 also goes high activating G10 which generates S11P-P. S11P-P enables G20 and RL4S-P activates G25 which enables gate G24 and activates gates G26, G39, and G40. The output of G26 disables G28, G30, G32, G36, and G38. G39 and G40 generate low outputs to interrupt level flip-flops U65 and activate gate G41. The high output of G41 is applied to interrupt level flip-flops U65 and enables gate G44. Inverter I9 inverts the output of G41, causing CYST-N (waveform M, figure 7) to go **low** which is routed to the Bus Controller alarm and INFIBUS timing circuit. At the same time, delay DLl delays S11P-P for 20 nsec which then activates G20. 15 inverts the output of G20 which activates G21. The output of G21 activates G24 which generates SEL4-N (waveform L, figure 7). The output of G24 also activates G27 which generates PCDI-P (waveform K, figure 7).

5-125. The Processor function, generating the level 4 interrupt, receives SEL4-N and the precedence pulse which causes SACK-N to go low. The Bus Controller alarm and INFIBUS timing circuit then generates RSAK-P (waveform N, figure 7). RSAK-P activates G44 which generates SCLK-P (waveform 0, figure 7) which is routed to the Bus Controller alarm and INFIBUS timing circuit, and triggers interrupt level flip-flops U65. Interrupt level flip-flops U65 generate ILOR-N and ILIR-N, a level four interrupt binary code, to the CPU, and INTR-N (waveform P, figure 7) to the Bus Controller alarm and INFIBUS timing circuit. INTR-N activates G43 and G19. The output of G43, RNIR-P (waveform Q, figure 7), is routed to the Bus Controller alarm and INFIBUS timing circuit and 18. 18 inverts RNIR-P, generating INAR-N (waveform R, figure 7), which is also routed to the Bus Controller alarm and INFIBUS timing circuit. The output of G19 disables gates G2, G5, G7, G12, G14 and G17. G9 is disabled and 4-bit latches U43 and U52 are cleared. G21 is disabled by the output of 11 which disables G.24. Disabling G24 causes SEL4-N to return to high.

5-126. The Processor function requesting the level 4 interrupt removes its request, SRL4-N (returns to high), and places its

data (device number) on the INFIBUS for the CPU. The CPU processes the data and generates the mask bits (waveform S, figure 7). in this case the level 4 interrupt was serviced and now level 3 is to be opened with the other levels closed. Mask bits LB15-P, LB13-P, and LB12-P are generated by the CPU presenting them to the mask flip-flops U71. The CPU then generates STAT-N (waveform T, figure 7) which is inverted by inverter 14. The output of 14 triggers the mask flip-flops U71. The mask flip-flops U71 are loaded with the mask bits and now Gl, G4, G11, G13 and G16 are disabled and G6 is enabled to be activated by a level 3 interrupt request (SRL3-N). The level 1, 2 and 3 interrupt requests (SRLl-N, SRL2-N and SRL3-N) are cycled in the same manner as the level 4 interrupt when the associated level is opened. The associated select signal, SELl-N, SEL2-N, or SEL3-N, will be generated and the interrupt level code, a combination of ILOR-N and ILIR-N, representing the level of interrupt being cycled will be coupled to the CPU. The mask flip-flops U71 will be loaded after every cycle, opening up the next lower priority level of interrupt. After the level 1 interrupt, SRLl-N request, level 4 will be opened with the other levels closed.

5-127. When the CPU requests to be selected for transferring the stored program data, the CPU generates SRLC-N, the lowest priority transfer request. SRLC-N is inverted by inverter 13 which activates gate G15. The output of G15 is applied to the 2D4 input of 4-bit latch U52 and also activates gate G9. The output of G9 triggers 4-bit latches U43 and U52 and the cycle is repeated as explained previously except that 4-bit latch U52 generates RLCS-P. G38 is activated by RLCS-P which enables gate G35.

5-128. When the Bus Controller alarm and INFIBUS timing circuit generates a CPU level 4 internal interrupts, DNUM-P is generated. If the level 4 interrupt is enabled by the mask flip-flops U71, DRUM-P activates gate Gl and the interrupt cycle is repeated as explained for the other levels of interrupts with the following exceptions: G2 Is activated and 4-bit latch U43 generates RPLS-P, G23 is activated which activates gates G37, G39, and G40, and G37 activates G27 which generates PCDI-P. NNTS-P is generated by interrupt level flip-flops U65 and routed to the Bus Controller alarm and INFIBUS timing circuit and ILOR-N and ILIR-N are generated and routed to the CPU representing a level 4 internal interrupt. No select signal (SELI-N through SEL4-N) is generated because the interrupt is being generated internally by the Bus Controller.

5-129. The CPU level 1 self-interrupt (DN3R-N) operates in the same manner as a CPU level 4 self-interrupt except, G16 is activated. The output of G16 activates G17 and 4-bit latch U52 generates REXS-P which activates G36. The output of G36 activates G37 and interrupt level flip-flops U65 generate NNTS-P (high), ILOR-N (high) and ILIR-N (high) which are routed to the CPU and represent a level 1 self-interrupt.

5-130. If two levels of interrupts are requested simultaneously, only the interrupt level which is enabled by the set mask flip-flop U71 is serviced. The same level of interrupts cannot be serviced successively because, after the first is cycled, mask flip-flops U71 close that level until all other interrupt levels are cycled. When an interrupt and a DDT request (SRLD-N) are requested simultaneously, the high priority DDT request will be serviced first. For example, if SRL4-N and SRLDLN are received, 4-bit latch U43 generates RLDS-P. RLDS-P is inverted by I6 which disables G23. The output of I6 activates G22, generating SELD-N, which selects the Processor function requesting INFIBUS access. When the DDT is completed, RL4S-P is generated again by 4-bit latch U43 and G25 is activated which activates G24. The output of G24, SEL4-N, selects the Processor function requesting a level 4 interrupt INFIBUS access.

5-131. If master inhibit, MINH-N, is generated by the Program Maintenance Panel, G18 will be disabled. With any interrupts received, NEXT-N is not generated and the interrupts will not be cycled.

5-132. BUS CONTROLLER A1A3A5 ALARM AND INFIBUS TIMING CIRCUIT.

5-133. General. The Bus Controller alarm and INFIBUS timing circuit monitors alarm inputs, generates internal interrupts, and generates assigned device numbers for the internal interrupts. When INFIBUS requests are cycled, the Bus Controller monitors the cycles and aborts them if they are not completed within predetermined time limits.

5-134. Detail Analysis (see figure 8). When 5 volts AC power is applied, the output of delay DL1 (waveform A, figure 9) remains low for 70 msec which activates gate G9. G9 generates the master reset pulse, MRES-N (waveform F, figure 9). The output of G9 is also coupled through driver DR3 which generates RSET-N (waveform J, figure 9). RSET-N resets flip-flop FF2 which enables gate G11. RSET-N also activates gate G14. The output of G14, RS-N, clears flip-flops FF3, FF5, FF6, and FF7. RSET-N also clears flip-flops FF11, FF12, FF13, and FF14. The Bus Controller service request select and interrupt circuit then generates SCRS-N (waveform K, figure 9) which clears the internal interrupt flip-flops U68 (FF7 shown typical). Also, RNIR-P (waveform L, figure 9), and INAR-N (waveform M, figure 9) are received from the Bus Controller service request selection and interrupt circuit RNIR-P activates gate G20 which generates DNOL-P and INAR-K disables gate G33.

5-135. Also, during the 70 msec low- output time of DLI, Schmitt trigger ST1 is activated. The output of ST1 (waveform B, figure 9) activates gate G2 which activates gate G3. The output of G3 triggers single shot SS1 and the 0 output of SS1 disables G2 which disables G3. The 1 output of SS1 (waveform C, figure 9), after 2.5 nmsec, triggers single shot SS2 and the 0 output of SS1 activates G2 which activates G3, triggering SS1 once again. The 1 output of SS2 (wave form D, figure 9) triggers single shot SS3 which activates gate G5 which presets flip-flop FF1. SS1 again resets in 2 5 msec which retriggers SS2. The output of SS2 then retriggers SS3. The cycle of retriggering SS3 occurs 28 times within the 70 msec time delay of DLl. The SS3 1 output (waveform E, figure 9) activates gate G10 and enables gate G8. Each time SS2 resets, G8 is activated which activates G9.

5-136. After 70 msec, the output of DLl goes high and ST1 is disabled which disables G2. In addition, the high output of DLl disables G9 which removes MRES-N and after 250 usec SS2 resets. The 0 output of SS2 (high) activates G8 which activates G9, generating MRES-N a second time for 190 msec. After 190 msec, SS3 resets and disables G8 which disables G9, removing MRES-N. The 1 output of SS3 (low) disables G10 and the low-to-high transition output of G10 activates the pulse generator C6 and R9, generating a 100 nsec pulse (waveform H, figure 9). The 100 nsec pulse activates G11 and DRl which generates the autoload pulse, ATLD-N (waveform I, figure 9).

5-137. Master reset, MRES-N can be generated at any time by touching the reset pushbutton on the Program Maintenance Panel. This generates REPB-N (waveform A, figure 10) which disables gate G5 and resets flip-flop FFl. The 1 output of FFl (low) activates G3 which triggers SSl. SS1 resets in 2.5 msec and the 1 output of SS1 (waveform B, figure 10) triggers SS2. The 1 output of SS2 (waveform C, figure 10) triggers SS3 and the 1 output of SS3 (waveform D, figure 10) enables G8 and G10. After 250 usec, SS2 resets and the 0 output of SS2 (low) **activates** G8 which activates G9, generating AIRES-S (waveform E, figure 10). FF1 remains reset until SS3 resets which activates G5 presetting FFl.

5-138. When any select cycle, DDT or interrupt, is being conducted by the Bus Controller service request select and interrupt circuit, S11P-P and PCDI-P are generated and routed to the Bus Controller alarm and INFIBUS timing circuit. S11P-P **is used** for setting a 2 usec time limit for the function to be selected and PCDI-P causes the precedence pulse, PCDB-P to be generated. With the selection in progress, S11P-P (waveform, A, figure 11) is generated which triggers single shot SS5, setting it for 2 usec. 20 to 30 nsec later,

PCDI-P (waveform B, figure 11) is generated which enables gate G12. PCDI-P is delayed by delay DL2 for 20 nsec and then activates G12. The output of G12 is inverted by inverter I2, generating PCDE-P which activates gate G13 and enables gate G24. The output of G12 is also delayed by delay DL3 for 50 nsec. The output of DL3 disables G13. G13 generates the precedence pulse PCDB-P (waveform C, figure 11). If SACK-N is not received from the selected Processor function within 2 usec, SS5 resets which activates G24. The output of G24 activates gate G23 which activates gate G19, generating SACK-N. SACK-N prevents the selected function from being serviced and aborts the cycle which clears the INFIBUS to allow other Processor functions to be serviced. Normally, within 25 to 350 nsec after PCDA-P is generated, SACK-N (waveform D, figure 11) is generated by the selected Processor function. Inverter 13 inverts SACK-N, generating RSAK-P (waveform E, figure 11) which is routed to the Bus Controller service request select and interrupt circuit. NSAK-N (waveform F, figure 11) is generated by the Bus Controller service request select and interrupt circuit and S11P-P and PCDI-P are removed. NSAK-N disables gate G25 and with PCDI-P removed, PCDE-P is also removed. RSAK-P also activates gate G21 which triggers single shot SS4 which will be set for 2 usec. The output of G21 also sets flip-flop FF9. The output of SS4 sets flip-flop FF8. The 0 output of FF8 is inverted by inverter 14 which enables G27.

5-139. 20 to 30 nsec after SACK-N is generated, the selected Processor function presents its data and 50 nsec later its strobe on the INFIBUS. The strobe, STRB-N (waveform G, figure 11), is inverted by inverter I6, generating RSTR-P. RSTR-P is inverted by inverter I8, generating RSTN-N. RSTN-N disables G26 and G21 which clears FF9. The 0 output of FF9 enables G26. 20 to 30 nsec after STRB-N is received, SACK-N is removed which removes RSAR-P and NSAK-N. If the service cycle is not completed within 2 usec after SACK-N is generated, SS4 resets which activates G27. The output of G27 is coupled through bus drive: receivers U28 which generates QUIT-N (waveform H, figure 11). QUIT-N aborts the service cycle and clears the INFIBUS to allow other functions to be serviced. Normally, within 2 usec, DONE-N (waveform I, figure 11) is generated by the serviced Processor function to indicate a completed data transfer. STRB-N is removed. The removal of STRB-N removes RSTR-P and RSTN-N which activates G26, clearing FF8. The 0 output of FF8 (high) is inverted by I4 which disables G27. The Bus Controller alarm and INFIBUS timing circuit returns to its initial conditions as explained previously.

5-140. With an interrupt being cycled by the Bus Controller service request selection and interrupt circuits, the Bus Controller alarm and INFIBUS timing circuits supports the cycle with additional signals. The norma1 internal SACK-N and QUIT-N timing is involved as explained previously and in addition, HOLD-N and DNOL-P are generated for the CPU to read the interrupting Processor function device number. As an interrupt is initiated, SCRS-N (waveform J, figure 11) is generated by the Bus Controller service request selection and interrupt circuit which resets the internal interrupt flip-flops U68. Also, at the same time, RNIR-P (waveform K, figure 11) and INAR-N (waveform L, figure 11) are removed. With RNIR-P low, G20 is disabled which removes DNOL-P (waveform M, figure 9). With INAR-N high, G33 is activated which sets FF11 and the 1 output of FF11 enables G31. CYST-N (waveform N, figure 11) is generated after S11P-P (waveform A, figure 11) and PCDI-P (waveform B, figure 11) are generated. G33 is disabled by CYST-N and the output of G33 enables G31. PCDB-P is generated at this time and G31 is activated. The output of G31 sets FF12 which enables gate G32, disables G33, and activates gates G34 and G37. The output of G34 sets FF13 and activates gate G40. G37 generates PSAK-N which disables G20. The 1 output of FF13 enables gates G35, G36 and G39 and activates gate G41 which activates G40. The output of G40, ONLN-P (waveform 0, figure 11), enables gate G28. ONLN-P is also inverted by inverter I5 which activates G30 and sets flip-flop FF10. The output of G30 is coupled through driver DR4, which generates HOLD-N (waveform P, figure 11). HOLD-N prevents the CPU from performing

a cycle with Core Memory. The 0 output of FF10 holds G30 activated.

5-141. The selected Processor function generates SACK-N (waveform D, figure 11), I3 inverts SACK-N and generates RSAK-P which is routed to the Bus Controller service request selection and interrupt circuit. The Bus Controller service request selection and interrupt circuit removes S11P-P, PCDI-P and CYST-N, and generates RNIR-P, INAR-N, INTR-N and SCLK-P. When PCDB-P goes low, G31 is disabled. The high output of G31 activates G32. The output of G32 clears FF11 which disables G31. RNIR-P enables G20 and INAR-N disables G33. The Processor function generating the interrupt presents its device number and strobe on the INFIBUS. The strobe, STRB-N (waveform G, figure 11), is inverted by 16 which generates RSTR-P. RSTR-P activates G36 which clears FF12, and disables G37. The 1 output of FF12 disables G32 and the 0 output enables G33. Disabling G37 causes PSAK-N to go high which activates G20. The output of G20), DNOL-P (waveform M, figure 11) is routed to the CPU. DNOL-P indicates to the CPU that the Processor function requesting INFIBUS access has placed its device number on the INFIBUS.

5-142. Normally, DONE-N (waveform I, figure 11) is generated by the selected Processor function to indicate a completed data transfer. DONE-N is inverted by inverter I9 which activates G39. Inverter I10 inverts the output of I9 and disables gate G38 and G34. The output of G39 sets FF14 and activates G40. The 1 output of FF14 enables G38, and the 0 output disables G41. When DONE-N returns to high, I9 disables G39 which disables G40, removing ONLN-P; The output of I10 activates G38 which clears FF13. The 1 output of FF13 disables G35, G36, G39 and G41 and clears FF14. The selected Processor function removes STRB-N, the QUIT-N timing is disabled, and the Bus Controller alarm and INFIBUS timing circuit is cleared to its initial condition as explained previously.

5-143. The external attention signal, EXAT-N, from the INFIBUS is generated by the Program Maintenance Panel to **interrupt** the CPU (CPU level 1 self-interrupt). EXAT-N sets flip-flop FF7 and the 1 output of FF7 is routed to its associated internal interrupt circuit to request a level 1 interrupt. This paragraph does not apply to TDCS.

5-144. LFRQ-N is generated by the PFD/Clock once every 40 msec and is used to update the calendar and clock program stored in Core Memory (CPU level 4 self-interrupt). If the LFRQ-N interrupt inhibit input, LFIN-N, from the Program Maintenance Panel is low, gate G1 is enabled. LFRQ-N triggers Schmitt trigger ST2 and the pulse generating network, C5 and R5, generates a 100 nsec pulse which activates G1. The output of Gl sets FF3. The 1 output of FF3 is routed to its associated internal interrupt flip-flop U68. The 0 output of FF3 activates gate G18 which generates DNUM-P. DNUM-P is routed to the Bus Controller service request selection and interrupt circuit to request a level 4 interrupt.

5-145. Power status, PWST-N (CPU level 4 self-interrupt), is held high to indicate regulated power is available. PFD/Clock logic activates this signal 2.2 to 3.0 msec before loss of regulation due to a power failure. The power fail interrupt has an inhibit input, PFIN-N, generated by the Program Maintenance Panel to inhibit a level 4 interrupt request (PFIN-N disables gate G7 when low). When PFIN-N is high, G7 is enabled. When there is loss of regulated power, PWST-N will be generated. PWST-N (waveform A, figure 12) is a 9.6KHz pulse train which activates ST1. The output of ST1 activates gate G6 which activates G7, G7 generates PF-N (waveform F, figure 12) which sets FF5. The 1 output of FF5 is routed to its associated internal interrupt flip-flop U68. The 0 output of FF5 activates G18 which generates DNUM-P a level 4 interrupt request. DNUM-P is routed to the Bus Controller service request selection and interrupt circuit. The level 4

interrupt will be completed within 300 nsec and, as explained previously, G2 is activated by the output of ST1 which activates G3. The output of G3 triggers SSl and its 1 output (waveform B, figure 12) triggers SS2 which triggers SS3. The 0 output of SSl activates G2 once again and the cycle repeats with every PWST-N pulse. SS2 resets in 250 usec and will be triggered again in 2.5 msec (waveform C, figure 12) which retriggers SS3 The 1 output of SS3 (waveform D, figure 12) enables G8 and every 250 usec SS2 resets which activates G8. The output of G8 activates G9 which generates MRES-N (waveform E, figure 12). MRES-N is generated for 2.5 msec and-is removed for 250 usec.

5-146. if regulated power is only lost momentarily and then recovers, G10 will be disabled after SS3 resets and the pulse generating network, C6 and R9, generates a 100 nsec pulse that generates the autoload, ATLD-N (waveform G, figure 12), pulse, as explained previously. ATLD-N is only generated if PRAL-N is low which is determined by a switch in the Program Maintenance Panel. If PRAL-N is high, the output of inverter I1 disables G11 and ATLD-N is not generated. If the PRIN-N, power restart interrupt inhibit signal, is not generated (high) by the Program Maintenance Panel, G4 will be enabled for a power restart interrupt. When pulse generating network C6 and R9 generates the 100. nsec pulse, G4 is activated which generates PR-N (waveform H, figure 12), setting FF6. The 1 output of FF6 is routed to its associated internal interrupt flip-flop U68. The 0 output of FF6 activates G18 which generates DNUM-P level 4 interrupt request. DNUM-P is routed to the Bus Controller service request selection and interrupt circuit.

5-147. DNUM-P and DN3R-N request a level 4 and a level 1 interrupt, respectively, and these interrupts are generated internally by the Bus Controller alarm and INFIBUS timing circuit. The interrupt cycles for these internal interrupts are similar to the Processor function interrupts except for the following. During the cycle, as PCDI-P (waveform B, figure 11) and CYST-N (waveform N, figure 11) are generated, NINT-N and NNTS-P (waveform Q, figure 11) are also generated by the Bus Controller service request selection and interrupt circuit. NINT-N enables gate G22 and when FF12 is set, G37 is activated which generates PSAK-N; PSAK-N disables G20 which removes DNOL-P. PSAK-N also activates G22 which activates G23. The output of G23 activates G19 which causes SACK-N (waveform D, figure 11) to go low. NNTS-P (waveform R, figure 11) goes high which enables G28. SCLK-P goes high triggering internal interrupt flip-flops U68 which sets the associated flip-flop as determined by which alarm (EXAT-N, LFRQ-N, PWST-N power fail, PF-N, or power restart, PR-N) has been generated. SCLK-P also activates gate G15 which activates gate G14. The output of G14, RS-N, clears FF3, FF5, FF6, and FF7. The outputs of the internal interrupt flip-flops U68 are routed to the bus drivers U58. Gate G16 receives the EXAT-N and LF-N outputs of internal interrupt flip-flops U68 which enables gate G17 of data bus driver U58. When ONLN-P (waveform 0, figure 11) is generated by G40, G28 will be activated which strobes data bus drivers U58 and enables gate G29. Also, I5 inverts ONLN-P which generates HOLD-N (waveform P, figure 11) via G30 and DR4. Data bus drivers U58 generate the device number, binary code of DBOO-N through DB03-N which represents the alarm generated, to the INFIBUS data lines. For an external attention, EXAT-N (CPU level I self-interrupt) or line frequency, LFRQ-N (CPU level 4 self-interrupt), DBOO-N goes low. For a power restart, PR-N, level 4 interrupt DB02-N is generated. For power fail, PF-N, level 4 interrupt DB0l-N is generated. G29 is activated after the delay of DL4 which generates STRB-N (waveform G, figure 11). When PSAK-N goes high G20 is activated and G22 is disabled. G20 generates DNOL-P, device number on line, which is routed to the CPU and G22 causes SACK-N to go high via G19 and G23. The remainder of the cycle is the same as explained previously.

5-148. When MRES-N is generated, RSET-N is generated which clears FF2. The 0 output of FF2 enables G10 to generate

ATLD-N. The 1 output of FF2 holds ST2 activated which prevents the LFRQ-N input from triggering ST2. During any interrupts cycled by the Bus Controller service request selection and interrupt circuit, INTR-N will be generated. INTR-N disables G15, and presets FF2. The 0 output of FF2 now disables Cl1 and the 1 output of FF2 enables ST2 to be triggered by LFRQ-N. FF2 will remain in this state until RSET-N is once again generated by MRES-N.

5-149. Oscillator Y2 generates a 25 MHz symmetrical square wave signal which is coupled to the INFIBUS by driver DR2, generating CLKA-N, CLKA-N is used by Processor functions for synchronizing and timing purposes.

5-150. CPU SEQUENCE REGISTER AND CONTROL STORAGE CIRCUIT.

5-151. General. The CPU sequence register and control storage circuit contains the CPU microprogram which controls the operation of the CPU. The sequence register addresses the control storage ROMS which generates microcode words which are stored in the CPU microcode register circuit.

5-152. Detail Analysis (see figure 13). When the master reset, MRES-N, is generated on the INFIBUS, the CPU control circuit generates RST2 -N which enables the clear (CLR) inputs of the sequence register/counters U43 and U44. On the next low to high transition of CKSR-N from the CPU central timing control circuit, the sequence register/counters U43 and U44 are clocked and cleared.

5-153. The sequence register/counters U43 and U44 are 4-bit presettable binary counters. They are cascaded to form an 8-bit presettable binary counter which counts from 0 to 255 (binary). When the CPU is in the run mode, the CPU control circuit generates RBFS-P which enables sequence register/counter U44 to count. On each low to high transition of CKSR-N, sequence register/counter U44 count increases by one. On the fifteenth count, the CRY output of sequence register/counter U44 goes high which enables sequence register/counter U43 to count. On the sixteenth count, sequence register/counter U43 count increases by one, the sequence register/counter U44 resets and the CRY output returns low. The cycle is repeated until a count of 255 is reached, then both sequence register/counters U43 and U44 reset to 0. If SCM1-N is generated, both sequence register/counters are prevented from counting.

5-154. The CPU microcode register circuit generates M04S-P through M11S-P which are applied to the parallel inputs of sequence register/counters U43 and U44. When the CPU control circuit generates SS07-N, the load inputs of sequence register/counters U43 and U44 are enabled. On the next low to high transition of CKSR-N, sequence register/counters U43 and U44 are clocked and loaded with the parallel data which specifies a jump address.

5-155. SOOS-P through SO7S-P from sequence register/counters U43 and U44, address the microcode words within the control storage ROMS. The control storage ROMS consist of nine 256 word 4-bit ROMS which generate 256 36-bit words. UBOO-P through UB35-P are routed to the CPU microcode register circuit for storage.

5-156. The microcode word is divided into 13 fields. The bit positions that make up the various fields are as follows:

BIT POSITION	FIELD
0-2	W
3	Z
4-7	L1
8-11	L2
12-15	M
16,17	Y
18,19	F
20-23	X
24,25	D
26,27	C
28-31	A
32	T
33-35	S

5-157. CPU MICROCODE REGISTER CIRCUIT.

5-158. General. The CPU microcode register circuit stores and generates the 36-bit microcode word for decoding by the various CPU circuits. The 36-bit microcode word controls all CPU generations. The CPU microcode register circuit receives the microcode word from the CPU sequence register and control storage circuit CPU emulation instruction register circuit, and CPU address recognition circuit stores the microcode word. The CPU microcode register circuit then generates control signals, specified by the microcode word, which are decoded by the CPU control circuit, CPU register file circuit, CPU emulation instruction register circuit, CPU central timing control circuit, CPU ALU circuit, CPU sequence register and microcode storage circuit, CPU ALU input multiplexer circuit, and CPU INFIBUS access circuit.

5-159. Detail Analysis (see figure 14). When the master reset pulse, MRES-N, is generated on the INFIBUS, the CPU control circuit generates RST2-N which activates gate Gl. Gl generates M32T-P which is routed to the CPU ALU circuit and CPU central Timing Control circuit.

5-160. UBOO-P, UBOl-P, UB02-P, UB18-P through UB25-P, and UB28-P through UB32-P, from the CPU sequence register and control storage circuit are routed to the respective data inputs of microcode registers U37, U38, and U40. UB03-P through UB17-P, UB20-P through UB23-P, UB26-P and UB27-P, and UB33-P through UB35-P are routed to the respective data inputs of microcode registers U33, U34, U35, U36, and U39 and CPU Central Timing Control circuit.

5-161. UB20-P through UB23-P from the CPU emulation instruction register circuit are wire-anded with UB20-P through UB23-P from the CPU sequence register and control storage circuit. UB02-P, UB28-P, and UB30-P from the CPU address recognition circuit are wire-anded with UB02-P, UB28-P, and UB30-P from the CPU sequence register and control storage circuit. UB04-P through UB15-P from the CPU emulation instruction register circuit are wire-anded with UB03-P through UB17-P from the CPU sequence register and control storage circuit.

5-162. CKML-P from the CPU central timing control circuit, and DNTS-P from the CPU control circuit activates gate G2 which generates CLRM-N. CLRM-N clears microcode registers U33 through U40.

5-163. CKML-P, from the CPU central timing control circuit, is also routed to the clock (CLK) inputs of microcode registers U37, U38, and U40 which loads the data inputs into the microcode registers U37, U38, and U40. CKME-P from the CPU central timing control circuit is routed to the clock (CLK) inputs of microcode registers U33 through U36 and U39 which loads the data input into the microcode registers U33 through U36 and U39.

5-164. Microcode registers U37, U38, and U40 generate the following: MOOT-P, MOlT-P M02T-P, MOOF-N, MOlF-N, M18T-P through M31T-P. If the QF output of microcode register U40 is low, Gl is activated which generates M32T-P.

5-165. Microcode registers U33 through U36, and U39 generate the following: M03S-P through M17S-P, M04R-N, MOSR-N, M12R-N through M14R-N, M20S-P through M23S-P, M22R-N, M23R-N, M26S-P, M27S-P, M33S-P through M35S-P, and M33R-N through M35R-N.

5-166. The CPU microcode register circuit routes the following bits to the CPU control circuit: M00F-N, MOOT-P, MOlF-N, MOLT-P, M22T-P through M25T-P, M23F-N, M22F-N, M20T-P, M2lT-P, M08S-P through MlOS-P, M12S-P through Ml5S-P, M12R-N, M14R-N, M33S-P through M35S-P, and M33R-N through M35R-N. The CPU microcode register circuit routes the following bits to the CPU emulation instruction register circuit for decoding: M18T-P, M19T-P, M03S-P through M11S-P, M04R-N, and M05R-N. M04S-P through Ml7S-P are routed from the CPU microcode register circuit to the CPU ALU input multiplexer circuit for decoding. M28T-P through M32T-P are routed from the CPU microcode register circuit to the CPU ALU circuit for decoding. M04S-P

through M13S-P are routed from the CPU microcode register circuit to the CPU sequence register and control storage circuit for decoding, M20S-P through M23S-P, M22R-N, and M23R-N are routed from the CPU microcode register circuit to the CPU register file circuit for decoding. M13R-N, M26S-P, and M27S-P are routed to the CPU carry and overflow circuit, and M02T-P and M32T-P are routed to the CPU central timing control circuit for decoding.

5-167. CPU CONTROL CIRCUIT.

5-168. General. The CPU control circuit decodes portions of the microcode word stored within the CPU microcode register circuit to control the operation of the various CPU circuits. The CPU control circuit controls the following circuits: CPU sequence register and control storage circuit, CPU address register circuit, CPU emulation instruction register circuit, CPU INFIBUS access circuit, CPU carry and overflow circuit, CPU central timing control circuit, CPU microcode register circuit, and the CPU address recognition circuit,

5-169. Detail Analysis (see figure 15). When the master reset pulse, MRES-N, is generated on the INFIBUS, MRES-N is inverted by inverter 19 which generates MRST-P. MRST-P disables data selector/multiplexer U47, and MRST-P is also routed to the CPU INFIBUS access circuit. Inverters 17 and 18 invert MRST-P which generates RSTl-P and RST2-P, respectively. RSTl-P is routed to the CPU central timing control circuit and RST2-P is routed to the CPU emulation instruction register circuit and CPU INFIBUS access circuit. In addition, RSTl-N resets flip-flops FF3 through FF5.

5-170. Data selector/multiplexer U48 decodes the binary-coded decimal at the A, B and C inputs which selects one of the eight data inputs (DO through D7). The selected input IS coupled to the Y output of data selector multiplexer U48 and the inverse of the selected input is coupled to the W output.

5-171. Gates G2 through G4 and inverters 13 and 14 decode inputs from the CPU microcode register circuit and CPU central timing control circuit to enable the binary decoder U32. When enabled, a binary-coded decimal at the A0 through A2 inputs of binary decoder U32 causes one of the seven outputs to go low.

5-l72. Gates G6 through G12 decode inputs from the CPU microcode register which controls the operation of the CPU address register circuit, CPU emulation instruction register circuit, CPU transmit register circuit and the CPU carry and overflow circuit.

5-173 . Data selector/multiplexer U47 decodes a binary-coded decimal at the A, B, and C inputs and selects one of eight data inputs, DO through D7. Gates G13 and G14 decode inputs from the CPU microcode register circuit and CPU control timing control circuit to preset flip-flop FFl.

5-174. Gates G16 through G18 decode inputs from the CPU microcode register circuit to generate STAT-N to the Bus Controller.

5-175. Flip-flops FF3 and FF5 are the CPU control register. FF3 is the halt buffer and FF5 is the run buffer. When FF3 is set, the CPU is in halt mode and when FF5 is cleared the CPU is in the run mode (performing operations). FF4 is the ALU buffer and when FF4 is set by ALU1-P, ALU1 -P is generated when a comparison test performed by the CPU ALU circuit is true. FF2 is the interrupt buffer which is cleared when interrupts are processed by the CPU.

5-176. Data selector/multiplexer U41 decodes the binary-coded decimal at A, B, C, and D inputs which selects one of the fourteen inputs (EO through E12 and E14). The selected input is inverted and coupled to the W output which generates CNDT-N.

5-177. CPU RECEIVE REGISTER CIRCUIT.

5-178. General. The CPU receive register circuit Interfaces the CPU with the INFIBUS data lines for the bidirectional transfer of

data. Data from the CPU transmit register circuit is transmitted onto the 1NFIBUS data lines or data from the INFIBUS is stored by the CPU receive register circuit for use by the CPU. Data stored by the CPU receive register circuit is routed to the CPU ALU input multiplexer circuit.

5-179. Detail Analysis (see figure 16). When master reset, MRES-N, is generated on the INFIBUS, the CPU transmit register circuit generates RSET-N which clears the receive registers U59, U69 and U79. Data bus driver/receivers U50, U60, U70 and U80 (inverter 12 typical) inverts the data, DB00-N through DB15-N, present on the INFIBUS data lines and generate DAOO-P through DA15-P which is routed to receive registers U59, U69 and U79. When the CPU is slaved to read data present on the INFIBUS data lines, the CPU address recgonition circuit generates RDCK-P which loads the receive registers U59, U69 and U79 with DAOO-P through DA15-P. The receive registers U59, U69 and U79 store the data and generate ROOS-P through R15S-P which are routed to the CPU ALU input multiplexer circuit for selection. ROOS-P is also routed to the CPU control circuit for testing.

5-180. When the CPU is slaved to read out data or when the CPU is slaving another Processor module and providing data, the CPU transmit register circuit generates TOOS-P through T15S-P. Inverters I2 through I17 invert TOOS-P through T15S-P and the data is routed to data bus driver/ receivers U5O, U60, U70, and U80. TOOR-N and T15R-N are also routed to the CPU emulation instruction register circuit to modify the fields within the microcode word. When the CPU address recognition circuit generates WOLN-P, the data bus driver/receivers U50, U60, U70 and U80 are strobed which generates DBOO-N through DB15-N.

5-181. CPU TRANSMIT REGISTER CIRCUIT.

5-182. Genera 1. The CPU transmit register circuit stores the data to be strobed to the INFIBUS data lines. It also receives data from the CPU ALU circuit and transmits data to the CPU receive register circuit, The data stored by the CPU transmit register circuit is also transmitted to the CPU ALU input multiplexer circuit for selection.

5-183. Detail Analysis (see figure 17). When master reset, MRES-N, is generated on the INFIBUS, inverter I1 inverts MRES-N and the output of I1 is inverted by inverter I2 which generates RSET-N. RSET-N clears the transmit shift registers U51 and U61 and is routed to and clears the CPU address recognition circuit, CPU address register circuit and CPU receive register circuit.

5-184. Data, LBOO-P through LB15-P, from the CPU ALU circuit, is routed to the parallel inputs of transmit shift registers U51 and U61. When the CPU control circuit generates STSL-P and STSR-P, a low to high transition of CKTR-N from the CPU central timing control circuit causes transmit shift registers U51 and U61 to be loaded with the parallel data, LBOO-P through LBl5-P. Transmit shift registers U51 and U61 store the data and generate T00S-P through T15S-P which are routed to the inputs of the transmit data bit selector U62 and to the CPU receive register circuit and CPU ALU input multiplexer circuit.

5-185. The CPU ALU input multiplexer circuit generates a binary code comprised of M12S-P through M15S-P which causes the transmit data bit selector to select one of the sixteen data bits, TOOS-P through T15S-P. If the selected bit position is high, the transmit data bit selector transmits BITl-N to the CPU control circuit.

5-186. When the CPU control circuit generates STSL-P, the S1 inputs of transmit shift registers U51 and U61 are disabled. This causes transmit shift registers U51 and U61 to shift the stored data to the left (QH to QA) on each successive low to high transition of CKTR-N.

5-187. When the CPU control circuit generates STSR-P, the SO **inputs** transmit shift registers U51 and U61 are disabled. This causes transmit shift registers U51 and U61 to shift the stored data to the right (QA to QH) on each successive low to high transition of CKTR-N.

5-188. The data recirculator U52 recirculates the data stored in transmit shift registers US1 and U61 when they are shifted left or right. When the CPU ALU input multiplexer circuit generates M12S-P and M13S-P, the 1C3 (T00S-P) and 2C3 (T15S-P) inputs of the data recirculator U52 are coupled to the 1Y and 2Y outputs, respectively. If transmit shift registers US1 and U61 are shifted to the right, T00S-P is coupled through data recirculator U52 to the SDRS (shift right) input of transmit shift register U51. If the transmit shift registers are shifted to the left, T15S-P is coupled through data recirculator U52 to the SDLS (shift left) input of transmit shift register U61. This causes the data stored in transmit shift registers U51 and U61 to be reentered into the respective transmit shift register.

5-189. When the CPU ALU input multiplexer circuit generates M12S-P, data recirculator U52 couples the 1Cl and 2C 1 inputs (CRYS-P) to the 1Y and 2Y outputs, respectively. When shifting transmit shift registers US1 and U61 left or right, each successive low to high transition of CKTR-N cause the associated data bit to assume the high or low level of CRYS-P.

5-190. When the CPU ALU input multiplexer circuit generates M13S-P, data recirculator U52 couples the lC2 and 2C2 inputs (ground) to the 1Y and 2Y outputs, respectively. When shifting transmit shift registers U51 and U61 left or right, each successive low to high transition of CKTR-N causes the associated data bit to return to logic 0.

5-191. With M12S-P and M13S-P both low, data recirculator U52 couples the 1C0 (Tl5S-P) and 2CO inputs (ground) to the 1Y and 2Y outputs, respectively. When shifting the transmit shift registers U51 and U61 left, each successive low to high transition of CKTR-N causes the associated data to return to logic 0. If shifting the transmit shift register U51 and U61 right, each successive low to high transition of CKTR-N causes the associated data to assume the present value of Tl5S-P.

5-192. CPU ADDRESS REGISTER CIRCUIT.

5-193. General. The CPU address register circuit interfaces the CPU with the INFIBUS address lines to transfer address information to or from the INFIBUS. Address information from the CPU ALU circuit is stored by the CPU address register circuit and transmitted to the INFIBUS address lines. The stored address information is also routed to the CPU ALU input multiplexer circuit for selection. Address information on the INFIBUS address lines is received by the CPU address register circuit and routed to the CPU address recognition circuit.

5-194. Detail Analysis (see figure 18). When master reset, MRES-N, is generated on the INFIBUS, the CPU transmit register circuit generates RSET-N. RSET-N clears address registers U6, U16, U26 and U36, and presets flip-flops FFl and FF2. A16R-N and A17R-N are generated by FFl and FF2, respectively, and routed to the CPU emulation instruction register circuit.

5-195. The CPU ALU circuit generates LB00-P through LB15-P which is routed to the inputs of the address registers U6, U16, U26 and U36. When the CPU control circuit generates ARCK-P, the address registers are clocked and loaded with the LB00-P through LB15-P address information. LB00-P is routed to the set and clear inputs of FF2 and LBOl-P is routed to the set and clear inputs of FFl. When the CPU control circuit generates SCM2-N, FFl and FF2 are set or cleared depending on the levels of LB00-P and LB0l-P.

5-196. The address information stored in address registers U6, U16, U26, and U36 is routed to bus drivers/receivers U10, U20, U30, and U40 (Gl shown typical). When ONLN-P is generated by the CPU INFIBUS access circuit, the address bus drivers/receivers are activated which generates AB00-N through AB15-N. Address registers U6, U16, U26 and U36 also generate A00S-P through A15S-P, which is routed to the CPU ALU input multiplexer circuit.

5-197. When an address is on the INFIBUS address lines, the address bus drivers/

receivers invert AB00-N through ABl5-N and generate BA0l-P through BAl5-P. The inverse of AB00-N is not used. BA01-N through BAO4-P are routed to the CPU emulation instruction register circuit and BAO5-P through BAl5-P are routed to the CPU address recognition circuit.

5-198. CPU ALU INPUT MULTIPLEXER CIRCUIT.

5-199. General. The CPU ALU input multiplexer circuit selects an operand (16-bit word) from either the CPU transmit register circuit, CPU receive register circuit, CPU address register circuit, or an 8-bit word from the CPU microcode register circuit.

5-200. Detail Analysis (see figure 19). Multiplexers U7, U8, U17, U18, U27, U28, U37 and U38 are each dual 4-line-to-l-line data selectors which selects data as determined by the binary code at the A and B inputs of the multiplexers. Ml6S-P and M17S-P from the CPU microcode register circuit are routed to all 8 multiplexers A and B inputs and determine which data is selected.

5-201. When M16S-P and M17S-P, from the CPU microcode register circuit are low, the ICO and 2C0 inputs of the 8 multiplexers are selected and coupled to the 1Y and 2Y outputs, respectively. This causes the R00S-P through Rl5S-P data from the CPU receive register circuit to generate Y00A-P through Y15A-P, as required, which are routed to the CPU ALU circuit.

5-202. When the CPU microcode register circuit generates M17S-P, the 1Cl and 2Cl inputs of the 8 multiplexers are selected and coupled to the 1Y and 2Y outputs, respectively. This causes the T00S-P through T15S-P data from the CPU transmit register circuit to generate Y00A-P through Y15A-P, as required, which are routed to the CPU ALU circuit.

5-203. When the CPU microcode register circuit generates Ml6S-P, the lC2 and 2C2 inputs of the 8 multiplexers are selected and coupled to the 1Y and 2Y outputs, respectively. This causes the A00S-P through A15S-P data from the CPU address register circuit to generate Y00A-P through Yl5A-P, as required, which are routed to the CPU ALU circuit.

5-204. When the CPU microcode register circuit generates Ml6S-P and M17S-P, the lC3 and 2C3 inputs of the 8 multiplexers are selected and coupled to the 1Y and 2Y outputs, respectively. This causes the M04S-P through M11S-P data from the CPU microcode register circuit to generate Y00S-P through YO7S-P and YO8S-P through Yl5S-P, as required, which are routed to the CPU ALU circuit. Y08S-P through Y15S-P are identical to Y00S-P through Yl5S-P in this case.

5-205. Gates Gl through G4 are enabled by Ml6S-P and M17S-P and all of the gates may be activated simultaneously or individually by M12S-P through M15S-P from the CPU microcode register circuit. M12S-P through M15S-P are also routed to the CPU transmit register circuit and M12S-P is also routed to the CPU ALU carry and overflow circuit.

5-206. If M12S-P and M13S-P are generated by the CPU microcode register circuit, G2 and G4 are activated which disables multiplexers U8, U18, U28, and U38. The M04S-P through M11S-P data from the CPU microcode register circuit generates Y08A-P through Yl5A-P, as required, and Y00A-P through YO7A-P will all be low.

5-207. If M14S-P and M15S-P are generated by the CPU microcode register circuit, Gl and G3 are activated which disables multiplexers U7, U17, U27, and U37. The M04S-P through M11S-P data from the CPU microcode register circuit generates Y00A-P through Y07A-P, as required, and Y08A-P through Y15A-P will all be low. Also, only gate Gl, G2, G3 or G4 will be activated and its associated multiplexers disabled. The M04S-P through MlSS-P data from the CPU microcode register circuit will be coupled through the multiplexers that are enabled.

5-208. CPU ALU CIRCUIT.

5-209. Genera 1. The CPU ALU circuit performs one of sixteen logical functions or one

of sixteen arithmetic functions on two parallel 16-bit words. One 16-bit word is from the CPU ALU input multiplexer circuit and the other 16-bit word is from the CPU register file circuit. Commands from the CPU microcode register circuit specify which logical or arithmetic function is to be performed on the two words by the CPU ALU circuit. The output of the CPU ALU circuit can be stored in the CPU transmit register circuit, CPU address register circuit, or CPU emulation instruction register circuit and/or the CPU register file circuit.

5-210. Detail Analysis (see figure 20). The ALU portion of the circuit consists of ALU's Ul, U11, U21, and U31. Each ALU performs 16 binary arithmetic operations or 16 Boolean (logical) operations on two 4-bit nibbles. The CPU ALU input multiplexer circuit generates YOOA-P through Y15A-P which are applied to the B inputs of the four ALU's Ul, U11, U21, and U31. The CPU register file circuit generates XOOS-P through Xl5S-P which are applied to the A inputs of the four ALU's Ul, U11, U21, and U31.

5-211. The CPU microcode register circuit generates M28T-P through M3lT-P which are applied to the S inputs of ALU U31 and ALU U21. These inputs specify which one of the 16 arithmetic or logical operations are to be performed. Drivers DRl through DR4 generate M28B-P through M31B-P which are applied to the S inputs of ALU Ul and ALU U11. These inputs specify which one of the 16 arithmetic or logical operations is to be performed. M32T-P from the CPU microcode register circuit is applied to the M input of the four ALU's Ul, U11, U21, and U31 and specifies whether an arithmetic or logical operation is to be performed. If M32T-P is high, logical operations are performed and if M32T-P is low, arithmetic operations are performed.

5-212. M28B-P, M29B-P, M31B-P and M32T-P arc routed to the CPU carry and overflow circuit and enables the circuit to generate a carry. When performing arithmetic operations, the CPU carry and overflow circuit generates CYIN-P when a carry condition is indicated and it is applied to the Cn input of ALU U31 and look-ahead carry generator U41. Each ALU Ul, U11, U21, or U31 indicates a carry condition by generating the X and Y outputs which are routed to the respective X and Y inputs of look-ahead carry generator U41. If ALU U31 indicates a carry condition, look-ahead carry generator U41. ALU Ul, U11, U21, or U31 indicates a carry condition by generating the X and Y outputs which are generator U41 generates CN08-N which is routed to ALU Ul1. If ALU Ull indicates a carry condition, look-ahead carry generator U41 generates CN12-N which is routed to ALU Ul. If ALU Ul indicates a carry condition, COUT-N is generated by ALU Ul and routed to the CPU carry and overflow circuit to indicate a carry condition.

5-213. ALU's U1, U11, U21 and U31 generate LBOO-P through LBl5-P which are routed to the CPU address register circuit, CPU transmit register circuit, CPU register file circuit, and CPU emulation instruction register circuit. LB12- P through LB15-P are also routed to the Bus Controller where they are used as mask bits when the Bus Controller and CPU are handling interrupts.

5-214. When two 16-bit words of equal magnitude are applied to the A and B inputs of the ALU's Ul, U11, U21, and U31 and a comparison operation is to be performed, each A = B output of the four ALU's Ul, Ull, U21, and U31 go high. The four A = B outputs are wire-anded together and ALU1-P is genera ted. ALU1-P is routed to the CPU control circuit to indicate equality.

5-215. CPU REGISTER FILE CIRCUIT.

5-216. Genera 1. The CPU register file circuit consists of twelve 16-bit registers constructed from twelve 4-by-4 flip-flop arrays. The twelve registers consist of the program counter (RO), seven general registers (Rl through R7), status register (R8), instruction register (R9), and file A (RA) and file B (RB) registers. Registers **RO through RB** are used internally for execution of the microcode program instructions. The CPU microcode register circuit: selects one of the twelve registers and data IS writtten into or read from the CPU ALU circuit.

5-217. Detail Analysis (see figure 21). Register files U5, U15, U25 and U35 are each one-quarter of registers R0 through R3. Register files U4, U14, U24 and U34 are each one-quarter of registers R4 through R7 and register files U3, U13, U23 and U33 are each one-quarter of registers R8 through RB.

5-2 18. The CPU ALU circuit generates LBOO-P through LBl5-P which are routed to the data inputs (D1 through D4) of the register files. LB00-P through LBO3-P are routed to the data inputs of register files U33, U34 and U35 which make up the first 4-bit positions of registers RO through RB. LB04-P through LB07-P are routed to the data inputs (Dl through D4) of register files U23, U24, and U25 which make up the next 4-bit positions of registers R0 through RB. LB08-P through LB11-P are routed to the data inputs (Dl through D4) of register files U13, U14, and U15 which make up the next 4-bit positions of registers RO through RB. LB12-P through LBl5-P are routed to the data inputs (Dl through D4) of register files U3, U4, and US which make up the most significant 4-bit positions of registers RO through RB.

5-219. M21T-P and M20T-P from the CPU microcode register circuit are routed to the WA and WB inputs of all twelve register files. A binary code from zero to three, of M20T-P and M2 IT-P, selects one-quarter of each of the twelve register files. Gates Gl, G2, and G3 decode M22F-N, M22T-P, M23F-N, and M23T-P and are activated by CKFS-P which generates WE03-N, WE47-N, or WE8B-N. The output of G1, G2, or G3 selects and clocks one of the three groups of the four register files (U3, U13, U23, U33; U4, U14, U24, U34; or U5, U15, U25, U35) and the data, LB00-P through LBl5-P, is written into the selected register. For example, to write into the general purpose register five (R5), the CPU microcode register circuit generates M20T-P, M22T-P, and M22F-N. With M20T-P high and M2lT-P low, all twelve register files select the second group of flip-flops (Rl, RS, and R9). M22F-N disables Gl and G3 and M22T-P enables G2. When the CPU central timing control circuit generates CKFS-P, G2 is activated which generates WE47-N. WE47-N clocks register files U4, U14, U24, and U34 to write the data into register R5.

5-220. To read data out of the register files, M20S-P and M21S-P from the CPU microcode register are routed to the RA and RB inputs of all twelve register files. A binary code from zero to three of M20S-P and M21S-P selects one of four groups of four flip-flops in each of the twelve register files. Gates G4, G5, and G6 decode M22R-N, M22S-P, M23R-N. and M23S-P and are activated by CKRD-P which generates RE03-N, RE47-N, or RE8B-N. The output of G4, G5, or G6 selects and clocks one of three groups of four register files (U3, U13, U23, U33; U4, U14, U24, U34; or U5, U15, U25, U35) and the data is read from the selected register. For example, to read from general purpose register five (R5), the CPU microcode register circuit generates M20S-P, M22S-P and M22R-N. With M20S-P high and M2lS-P low, all twelve register files select the second group of flip-flops (Rl, R5, and R9). M22R-N disables G4 and G6 and M22S-P enables G5. When the CPU central timing control circuit generates CKRD-P, G5 is activated which generates RE47-N. RE47-N causes the output data (Ql through Q4) of register files U34, U24, U14, and U4 to be generated.

5-221. Inverters 11 through 116 and gates G7 through G22 form latches which latch on low inputs. The Q outputs of the register files are normally high and the inverters activate the gates which holds X00S-P through Xl5S-P high. When a selected registers Ql output goes low, it is inverted by 11 which disables G7. When the register is no longer selected, the Ql output returns to high but G7 holds the output, X00S-P, low via Il. When XSET-N is generated by the CPU central timing control circuit all of the latches are cleared. For example, XSET-N activates G7 and the high output of G7 is inverted by 11 which holds G7 activated,

5-222. When a register is selected to read out data, X00S-P through Xl5S-P are generated to the CPU ALU circuit. Xl5S-P is also routed to the CPU carry and overflow

circuit and is inverted by inverter 116 which generates X1SR-N .

5-223. CPU CARRY AND OVERFLOW CIRCUIT.

5-224. General. The CPU carry and overflow circuit indicates when a carry and/or overflow condition has occurred. It receives control data from the CPU microcode register circuit, CPU ALU circuit, CPU transmit register circuit, CPU register file circuit, CPU ALU input multiplexer circuit, and CPU control circuit. It indicates a carry condition to the CPU ALU circuit, CPU transmit register, and CPU control circuit. Also, an overflow condition is indicated to the CPU control circuit.

5-225. Detail Analysis (see figure 22). When the CPU ALU circuit generates M32T-P gate G7 is enabled and inverter I3 inverts M32T-P which disables gate G9. When the CPU microcode register circuit generates M27S-P, gate G8 is enabled and when the CPU central timing control circuit generates CKTS-P, G7 is activated. G7 activates G8 which resets flip-flops FFl and FF2.

5-226. When COUT-P is generated by the CPU ALU circuit gate G10 is enabled and inverter I5 inverts COUT-P which disables G10 and gate G13. When the CPU ALU circuit generates M29B-P, gates G3 and G5 are activated. G3 activates gate G2 which generates CYIN-N to the CPU ALU circuit and G5 activates G10 which disables the clear input of FFl. Invetter I4 inverts the output of G10 and enables the set input of FFl. When the CPU control circuit generates TSHF-P, gate G11 is activated which enables gate G12.

5-227. When the CPU central timing control circuit generates CKTS-P, G12 is activated. Inverter I6 inverts the output of G12 and provides a high at the T input of FFl. When CKTS-P is removed, G12 is disabled and inserter 16 provides a low to the T input of FFl. The high-to-low transition at the T input of FFl triggers and sets FFl. FFl generates CRYS-P which is routed to the CPU transmit register circuit and the CPU control ciriuit.

5-228. When G3 is activated gate G4 is enabled and when G9 is activated, G4 is activated . The output of G4 and the output of I5 activates G10 when COUT-P from the CPU ALU circuit is low. This condition also enables the set input of FFl, hence, FF1 is set as explained previously.

5-229. When G11 is activated and T00S-P and STSR-P are generated by the CPU transmit register circuit and M12S-P is generated by the CPU ALU input multiplexer circuit, G10 is activated. This enables the set input of FFl, hence, FFl is set as explained previously.

5-230. When G11 is activated and the CPU transmit register circuit generates Tl5S-P and STSL-P G10 is activated which enables the set input of FF1. FF1 is set as explained previously.

5-231. When G7 is activated, gate G6 is enabled and when the CPU microcode register circuit generates M26S-P gate Gl is enabled and G6 is activated which presets FFl. The output of FF1, CRYS-P, activates Gl which activates G2. The output of G2, CYIN-N, is routed to the CPU ALU circuit.

5-232. When G5 is activated, the output of G5 activates gate G14 which enables gate G13. When the CPU register file circuit generates Xl5S-P, G13 is activated which activates gate G16. The output of G16 enables the set input of FF2. When a high-to-low transition output of 16 occurs, FF2 is set which generates OVFS-P. OVFS-P is routed to the CPU control circuit to indicate an overflow condition.

5-233. Inverter I7 enables gate G15 and when the CPU ALU circuit generates COUT-P and LBl5-P, G5 is activated and FF2 is enabled and set as explained previously.

5-234. When G11 is activated, gate G18 is enabled and when the CPU transmit register circult generates T14S-P, gate C17 is activated which enables G18. When the CPU transmit register circuit generates STSL-P, G18 is activated and FF1 is set as explained previously.

5-235. CPU EMULATION INSTRUCTION REGISTER CIRCUIT.

5-236. General. The CPU emulation instruction register circuit modifies fields of the microcode word stored in the CPU microcode register circuit. It also stores data from the CPU ALU circuit. This stored data addresses the data tables which are comprised of two ROM's. The outputs of the data tables modify the M, Ll, and L2 fields of the microcode word stored in the CPU microcode register circuit.

5-237. Detail Analysis (see figure 23). When the master reset pulse, MRES-N, is generated, the CPU control circuit generates RST2-N which clears emulation registers Ul and US and emulation register/counter U3.

5-238. LBOO-P through LB15-P from the CPU ALU circuit are routed to the data inputs of emulaation registers U1 and US and emulation register/counter U3. Emulation registers Ul and US are clocked by SETE-P from the CPU control circuit which loads them with LB04-P through LB15-P, as required. Emulation register/counter U3 is loaded with LBOO-P through LB03-P when the CPU control circuit generates LCLD-N which enables the load (LD) input of emulation register/counter U3. The low-to-high transition of CKTR-N from the CPU central timing control clocks the emulation register/ .counter U3.

5-239. When the CPU control circuit generates TSE-IF-P, the emulation register/ counter U3 is enabled to count by one on each low-to-high transition of CKTR-N. Emulation register/counter U3 counts from the preloadecd binary count (determined by LBOO-P through LB03-P) to binary 15 and generates EMAX-P which is routed to the CPU control circuit. On the sixteenth count the emulation register/counter U3 resets to zero.

5-240. Emulation registers Ul and U5 and emulation register/counter U3 generate EOOS-P through E15S-P which are routed to the table ROM address multipiexers U2 and U4. E03S-P, E07S-P, E11S-P, and E14S-P are also routed to the CPU control circuit. E11S-P is also routed to the CPU INFIBUS access circuit. When E12S-P and E13S-P, from emulation register Ul are low, gate Gl is activated generating DTOA-P which is routed to the CPU control circuit.

5-241. EOOS-P through E03S-P are also routed to the CO through C3 inputs of the X field modification multiplexer U15. Also, E04S-P through E07S-P are routed to the BO through B3 inputs of the X field modification multiplexer U15. BAOl-P through BAO4-P from the CPU address register circuit are routed through four spare INFIBUS lines, between the CPA A1A3A7 and CPB A1A3A6, to the A0 through A3 inputs of the field modification multiplexer U15.

5-242. The X field modification multiplexer U15 selects one of the three groups of data (EOOS-P through E03S-P; E04S-P through E07S-P; or BAOl-P through BAO4-P) as determined by the levels of Ml8T-P and M19T-P from the CPU microcode register circuit. M18T-P and M19T-P are routed to the select inputs (SO and S1 of X field modification multiplexer U15. When M18T-P and M19T-P are both low, gate G2 is disabled which disables X field modification multiplexer U15 and associated outputs (FO through F3) are all high.

5-243. When M18T-P is high, G2 is activated which enables X field modification multiplexer U15. Also, M18T-P causes X field modification multiplexer U15 to couple EOOS-P through CO3S-P to the FO through F3 outputs. UB20-P through UB23-P assume the logic levels of data EOOS-P through E03S-P and are routed to the CPU microcode register circuit to modify the X field of the microcode word.

5-244. When M19T-P is high, G2 is activated which enables X field modification multiplexer U15. Also, M19T-P causes X field modification multiplexer U15 to couple E04S-P through E07S-P to the FO through F3 outputs. UB20-P through UB23-P assume the logic levels of data E04S-P through E07S-P and are routed to the CPU microcode register circuit to modify the X field of the microcode word.

5-245. When M18T-P and M19T-P are both high, G2 is activated which enables X field modification multiplexer U15. Also, M18T-P and M19T-P cause X field modification multiplexer U15 to couple BAOl-P through BAO4-P to the FO through F3 outputs. UB20-P through UB23-P assume the logic levels of data BAOl-P through BAO4-P and are routed to the CPU microcode register circuit to modify the X field of the microcode word.

5-246. When the CPU control register is addressed, the CPU address register circuit generates BAOl-P through BAO4-P which activates gate G3. The output of G3, BADF-P, is routed to the CPU address recognition circuit which allows the control register to be selected.

5-247. Table ROM address multiplexers U2 and U4 select either EOOS-P through E03S-P, E04S-P through E07S-P, E08S-P through E11S-P, or E12S-P through E15S-P, as determined by the levels of M08S-P and MOSS-P. The outputs (1Y and 2Y) of table ROM address multiplexer-s U2 and U4 are used to address the data table ROM's 11 and 12 (U12 and U13), and are also inputs to the M field modification multiplexer U11. M06S-P, M07S-P, M10S-P, and M11S-P from the CPU microcode register circuit are also used to address the data table ROM's 11 and 12 (U12 and U13).

5-248. The Ll field modification multiplexer U21 selects either TOOR-N and T15R-N from the CPU receive register circuit, A16R-N and A17R-N from the CPU address register circuit, or OVFS-P, CRYS-P and ONAR-N from the CPU control circuit. CPU1-P and CPUO-P from the Bus Controller A1A3AS are always low and are inputs to L2 field modification multiplexer U14. ILlR-N and ILOR-N from the Bus Controller represent the interrupt level being cycled by the Bus Controller and CPU. ILOR-N and ILlR-N are also inputs to L2 field modification multiplexer U14.

5-249. Gates G1 through G4 decode M03S-P M04S-P, MOSS-P, and M04R-N. Gl through G3 determine which data is to be coupled through M field modification multiplexer U11 and L2 field modification multiplexer U14. G4 disables the data table ROM's 11 and 12 (U12 and U13).

5-250. CPU ADDRESS RECOGNITION CIRCUIT.

5-251. General. The CPU address recognition circuit recognizes the CPU address and enables read or write operations with internal registers of the CPU. The CPU address register circuit senses the address on the INFIBUS and enables the CPU receive register circuit to place data on the INFIBUS or read data from the INFIBUS.

5-252. The CPU is assigned address FFxy l6 where x is 0 or 1 and y is an even number from 016 to E16 which allows selecting 1 of the 12 addressable registers in the CPU register file circuit or the control register in the CPU control register circuit. The registers addresses are as follows:

REGISTER	ADDRESS
Register 1 (RO)	FF00 16
Register 2 (Rl)	FF04 16
Register 3 (R2)	
Register 4 (R3)	FF08 16
Register 5 (R4)	16
Register 6 (R5)	$FFOA_{16}$
Register 7 (R6)	$FFOC_{16}$
Register 8 (R7)	FF10 16
Register 9 (R8)	16
Register 10 (R9)	FF14 16
Register 11 (R10)	
Register 12 (11)	FF16 16
*Control Register (R15)	FFlE 16;

*Note: Located in CPU control register circuit.

5-253. Detail Analysis (see figure 24). When master reset, MRES-N, is generated on the INFIBUS, the CPU control circuit generates MRST-P which activates gate G11. The output of G11 resets flip-flop FF2 and clears flip-flop FF1. When STRB-N: is high, STRR-P from the CPU INFIBUS access circuit is low which resets flip-flop FF3. The 1 output of FF3 (low) sets flip-flop FF3 which enables gates G10 and G18.

5-254. When the CPU address is on the INFIBUS address lines, BAO8-P and BA09-P

activate gate G8, BAl0-P through BA12 -P activate gate G6, and BA13-P through BAl5-P activate gate G4. CPU1-P and CPUO-P from the Bus Controller are always low and when BAO6-P and BAO5-P are low, the output of gates G12 and G14 are high. BAO7-P is also low and the output of inverter I1 is high.

5-255. The high outputs of G4, G6, G8, I1, G12 and G14 are coupled through driver DR1 which generates SARC-P. SARC-P signifies the address is valid and the set input of FF3 is enabled. The function slaving the CPU then generates STRB-N which is inverted by inverter I3. The output of I3 is coupled through driver DR3. At the same time, STRR-P from the CPU INFIBUS access circuit is generated which disables the reset input of FF3. Inverter 14 inverts the output of DR3 and generates STRC-N which triggers and sets FF3. Setting FF3 signifies that address recognition has occurred.

5-256. When the control register of the CPU is addressed, the CPU emulation instruction register circuit generates BADF-P which enables gate G16 when address recognition occurs the 1 output of FF3 activates G16 and G18. The output of G16 generates WARC-P which clocks the control register in the CPU control circuit. The output of G18 activates G20 which generates CKEN-P to the CPU central timing control circuit. Inverter I5 inverts WARC-P which activates gate G7. The 1 output of FF2 activates G9 and its output is coupled through driver DR2 which generates DONE-N. The output of G7 triggers and sets FF2. The CPU central timing control circuit now generates CMEN-N which clears FF4 and disables G18 which causes CKEN-P to be removed. Delay DLl delays the 1 output of FF2 for 50 nsec and then the output of DLl activates G11. The output of G11 disables G9 (DONE-N returns to high) and resets FF2. The function addressing the CPU senses the removal of DONE-N and removes STRB-N causing the CPU INFIBUS access circuit to remove STRR-P which resets FF3.

5-257. When the CPU is in the halt mode, the CPU registers can be addressed. RBFR-N from the CPU control circuit is high which enables gates G10, G13, and G15. When a register is addressed to have data written into it, the CPU INFIBUS access circuit generates WRIT-P which enables gates G10, G24, and G25. Inverter 16 inverts WRIT-P which disables gates G1 and G23. When Address recognition occurs, the 1 output of FF3 activates G10, G13, and G18 and enables G15. The output of Gl0 activates gate G3 which generates RDCK-P. RDCK-P causes the CPU receive register circuit to read data from the INFIBUS data lines. The output of G13 activates G24 and G25 and the CPU microcode register circuit receives only UB02-P (output of G23). UB02-P modifies the microcode word which allows the data to be written into the selected register of the CPU register file circuit. The output of G 18 activates G20 which generates CKEN-P to the CPU central timing control circuit which initiates the cycle of writing data into the selected register. The CPU central timing control circuit then generates CMEN-N which clears FF4 and disables G10 and G18 causing CKEN-P and RDCK-P to be removed. The CPU central timing control circuit generates Z150-N 150 nsec later which activates gate G22. The output of G22 activates Gl5 and the output of G15 activates G7 which triggers and sets FF2. The 1 output of FF2 activates G9 and the output of G9 is coupled through DR2 which generates DONE-N. The output of DLl activates G11, 50 nsec later which disables G9 and resets FF2. Disabling G9 removes DONE-N and, as explained previously, FF3 is cleared.

5-258. When a register is addressed to have its data read (placed on INFIBUS), the operation is similar to writing data into the register except, WRIT=-? is not generated by the CPU INFIBUS access circuit. G10, G24 and G25 are disabled and the output of I6 enables Gl and G23. When G13 is activated, Gl and G23 are activated. The output of G1 activates gate G2 which generates WOLN-p to the CPU receive register circuit which enables the data to be placed on the INFIBUS data lines. With G23 activated, the CPU microcode register circuit receives

only UB28-P and UB30-P which signifies a read operation.

5-259. When the CPU is in the run mode, the CPU control circuit generates RBFR-N and RBFS-P. RBFR-N disables G10, G13, and G15 which prevents reading from or writing into the registers. RBFS-P activates gate G21 which activates G20. The output of G20, CKEN -P, is routed to and allows the CPU central timing control circuit to continue cycling.

5-260. To stop cycling the CPU when an INFIBUS access request cycle is to be performed by the CPU INFIBUS access circuit, SCE3-P is generated by the CPU control circuit which enables gate G19. When the INFIBUS access cycle is initiated, the INFIBUS access circuit generates BSYR-N which activates gate G17. The output of G17 activates G19 which disables G21. The output of G21 disables G20 which removes CKEN-P for the time BSYR-N is generated.

5-261. When the INFIBUS access request by the CPU INFIBUS access circuit is to allow the CPU to slave another Processor function and read data from it, the CPU INFIBUS access circuit generates RCKL-N. RCKL-N activates G3 which generates RDCK-P. RDCK-P causes the CPU receive register circuit to read data from the INFIBUS data lines.

5-262. When the INFIBUS access request by the CPU INFIBUS access circuit is to allow the CPU to slave another Processor function and present data to it, the CPU INFIBUS access circuit *generates MWOL-N. MWOL-N activates G2 which generates WOLN-P which causes the CPU receive register circuit to present data to the INFIBUS data lines.

5-263. During read or write INFIBUS access request cycles the slaved Processor function generates DONE-N. DONE-N is inverted by inverter I2 which generates and routes DUNP-P to the CPU INFIBUS access circuit.

5-264. DNOL-P from the Bus Controller is normally high and when the CPU is handling interrupts with the Bus Controller, DNOL-P goes low. When DNOL-P goes low, FFl is set and the 1 output of FFl enables gate G5. When the device number of the interrupting Processor function is placed on the INFIBUS data lines, the Bus Controller generates DNOL-P (high) which activates G5. The output of G5 activates G3 which generates RDCK-P. The output of G5 also activates G7 which sets FF2 and DONE-N is generated as explained previously.

5-265. CPU INFIBUS ACCESS CIRCUIT.

5-266. General. The CPU INFIBUS access circuit performs the function of gaining access to the INFIBUS, on the lowest priority direct data transfer level (SELC-N), to enable the CPU to transfer instructions. Control data from the CPU microcode register circuit specifies a read or write operation to the CPU INFIBUS access circuit and the CPU control circuit instructs the CPU INFIBUS access circuit when to initiate an INFIBUS access request.

5-267. Detail Analysis (see figure 25). When master reset, MRES-N, is generated on the INFIBUS, the CPU control circuit generates MRST-P and RST2-N. MRST-P activates gate G4 and the output of G4 clears the command register, U53. RST2-N clears flip-flops FF2, FF3, FF4 and FF5.

5-268. M08S-P, MOSS-P and M10S-P from the CPU microcode register circuit and E11S-P from the CPU emulation instruction register circuit are the command data bits that are stored in command register U53. M08S-P is generated by the CPU microcode register circuit when the CPU reads from an addressed location. M08S-P is routed to the A input of command register U53 and activates gate G3. The output of G3 generates a high to the D input of command register U53.

5-269. MOSS-P is generated by the microcode register circuit when the CPU writes into an addressed location. M09S-P is

routed to the B input of command register U53 and also activates G3 which provides a high to the D input of command register U53.

5-270. M10S-P is generated by the CPU microcode register circuit and E11S-P is generated by the OPIT emulation instruction register circuit when the CPU is to perform a byte read or write operation M10S-P and E11S-P activate gate Gl which provides a high to the C input of the command register U53.

5-271. When the CPU is to gain access to the INFIBUS, the CPU control circuit generates SCMD-P and SCMN-N. SCMD-P clocks and loads command register US3 with the desired command data. SCMN-N from the CPU control circuit ensures that FF5 is cleared and the 0 outputs of FF3, FF4 and FF5 activate gate G21. The output of G21 enables gate G11.

5-272. With a read or write command loaded into command register U53, the QD output is high and the QD, BSYR-N, output is low. The high QD output enables gates G6, G9, and G20 and activates G11. The output of G11 disables gates G12 and G15 and sets FF2. The 1 output of FF2 activates G9 which enables G12 and G15. The output of G9 also activates gate G10 which generates SRLC-N (waveform A, figure 27). SRLC-N is also inverted by inverter 16 which enables G14.

5-273. The Bus Controller senses SRLC-N and after granting higher priority INFIBUS access requests, the Bus Controller selects the CPU by generating SELC-N (waveform B, figure 27) and PCDA-P (waveform C, figure 27). SELC-N disables G11 which activates G12 and enables G15. The output of G12 disables gate G13 which blocks (traps) the precedence pulse.

5-274. The precedence pulse, PCDA-P, activates G15 which sets FF3. The 1 output of FF3 enables G16 and G17 and the 0 output of FF3 disables G4, G10, G19 and G21. Driver **DR1** is also activated by the 0 output of FF3 which generates SACK-N (waveform D, figure 27). Disabling G10 removes SRLC-N and enables G20. The output of G21 also disables G11.

5-275. The Bus Controller senses SACK-N and removes SELC-N. G15 is disabled when PCDA-P is removed and the output of G15 (high) activates G16. The output of G16 clears FF2 and the 0 output of FF2 (high) enables gate G8 and activates G17. The output of G17 sets FF4. The 1 output of FF4 activates G8 and enables gates G14 and G18. The output of G8 is inverted by inverter 13 which activates G6. The output of G6, ONLN-P (waveform E, figure 27), strobes the bus drivers/receivers U49, gates G5, G7 and G19. ONLN-P is routed to the CPU address register circuit which strobes the address onto the INFIBUS address lines.

5-276. If command register U53 is loaded with a write command, the QB output (high) enables G7 and the QB output (low) enables gate G2 which are activated by the output of G6. The output of G7 MWOL-N (waveform F, figure 27) is routed to the CPU address recognition circuit which causes data to be strobed onto the INFIBUS data lines. G2 generates RITE-N (waveform G, figure 27), on the INFIBUS to indicate that the data provided is to be written into the addressed location. If a byte of data is to be transferred, the QC output of command register U53 is low and bus drivers/receivers U49 also generate BYTE-N (waveform H, figure 27) to indicate a byte is to be transferred.

5-277. If a read command is loaded in command register U53, the QA output is high which enables G5 to be activated by the output of G6. The output of G5 sets FFl. BYTE-N will also be generated, as explained previously, if byte transfers are to be performed.

5-278. The output of G8 is also delayed by DL2 for 50 nsec and then causes the bus drivers/receivers to generate STRB-N (waveform I, figure 27) and STRB-P (waveform J, figure 27). STRB-P activates G18 and is inverted by inverter I5. The output of I5 disables G17. The output of G18 clears FF3 and the 0 output of FF3 disables DR1,

which removes SACK-N, and enables G10, G19, and G21.

5-279. If the transfer of data on the INFIBUS is not completed within'2 usec after STRB-N is generated, the Bus Controller generates QUIT-N. QUIT-N is inverted by inverter I4 which activates G19. The output of I4 is also inverted by inverter 17 which disables G17 and G20. The output of G19 sets FF5 which enables G4 and also routes BAES-P to the CPU control circuit to indicate an abort condition. The 0 output of FF5 clears FF4 and the 0 output of FF4 activates G4. The 1 output of FF4 disables G8 and G14. The output of G4 clears the command register U53 which frees the INFIBUS.

5-280. Normally, before 2 usec after STRB-N is generated, the addressed Processor function responds by generating DONE-N which indicates a completed data transfer. The CPU address recognition circuit senses DONE-N and generates DUNP-P (waveform K, figure 27). DUNP-P activates G4 and G5 and is inverted by inverter 12. The output of G4 clears command register U53 which frees the INFIBUS. The output of 12 disables G14 and G20.

5-281. If a read command is loaded in command register U53, G5 is enabled as explained previously. DUNP-P now activates G5 and G4. The output of G5 sets flip-flop FFl which generates RCLK-N (waveform L, figure 27). RCLK-N is routed to the CPU address recognition circuit which causes the CPU to load the data into receive register. The output of G4 clears the command register which frees the INFIBUS.

5-282. CPU CENTRAL TIMING CONTROL CIRCUIT.

5-283. General. The CPU central timing control circuit generates the timing pulses required by the various CPU circuits in executing the stored microcode program. When the CPU is in the halt mode, the CPU address recognition circuit triggers the CPU central timing control circuit to cycle when the CPU is addressed to read data from or write data into a register. When the CPU is in the run mode, the CPU central timing control continuously cycles to execute the stored microcode program.

5-284. Detail Analysis (see figure 27). When the master reset pulse, MRES-N, is received from the INFIBUS, the CPU control circuit generates RSTl-N (waveform A, figure 28) and the CPU microcode register circuit generates M32T-P (waveform B, figure 28). RSTl-N presets flip-flop FFl and M32T-P enables gate G4. The 1 output of FFl activates gates G2 and G5, The output of G2 is coupled through driver DRl and G5 generates CKOO-P (waveform C, figure 28). CKOO-P is routed to the CPU control circuit. The low output of DRl is inverted by inverter 15 which generates CKME-P (waveform D, figure 28). Inverter 18 inverts CKME-P generating CMEN-N (waveform E, figure 28) which resets FF4 and is routed to the CPU address recognition circuit. CMEN-N also disables G5 which removes CKOO-P (waveform C, figure 28). The pulse width of CKOO-P is determined by the inherent delays of G2, DRl, 15, and 18.

5-285. Delay DL3 delays the low output of DR1 15 nsec and the delayed output (15) is then inverted by inverter 12. The output of 12, CKML-P (waveform F, figure 28), is routed to the CPU microcode register circuit and enables gate G6.

5-286. After the 30 nsec delay of DL3, the low output of DL3 (30) is inverted by inverter 16. The output of 16, CKRD-P (waveform G, figure 28)) is routed to the CPU control circuit and CPU register file circuit. CKRD-P also enables G4 and activates G6. The output of G6, XSET-N (waveform H, figure 28), is routed to the CPU register file circuit.

5-287. After the 45 nsec delay of DL3, the low output of DL3 (45) is inverted by inverter 13. The output of 13 activates G4 which disables G2 and G5. The high output of G2 is coupled through DRl. The high output of DRl is inverted by 15 which removes CKME-P (waveform D, figure 28) and is inverted by I8 which ensures FF4 is reset and generates CMEN-N (waveform E, figure 28).

5-288. After the 60 nsec delay of DL3, the low output of DLl (60) is inverted by inverter I7 which generates C60A-P (waveform I, figure 28). C60A-P activates gate G3 which resets FF1 which disables G2. At the same time, the high output of DRl which has been delayed 15 nsec by DL3 is inverted by I2 which removes CKML-P. With CKML-P removed, G6 is disabled which removes XSET-N (waveform H, figure 28). The high-to-low transition output of 12 also triggers and sets flip-flop FF3 which generates CKTS-P (waveform K, figure 28) and CKTR-N (waveform L, figure 28). CKTS-P is routed to the CPU control circuit and CKTR-N is routed to the CPU control circuit, CPU emulation instruction register circuit, and CPU transmit register circuit.

5-289. After the 75 nsec delay of DL3, the low output of DL3 (75) is inverted by inverter I4. The output of I4, CKDO-P (waveform J, figure 28), is routed to the CPU control circuit. At the same time, the high output of DKl which has been delayed 30 nsec by DL3 is inverted by 16 which removes CKRD-P (waveform G, figure 28) and disables G4 and G6. The output of G4 enables G2 and G5 and disables G6 which removes XSET-N. The high-to-low transition output of 16 triggers and sets FF4. The output of FF4, CKSR-N (waveform M, figure 28) is routed to the CPU sequence register and microcode storage circuits.

5-290. After the 90 nsec delay of DL3, the low output of DL3 (90) disables G3 which enables G2. If the CPU microcode register circuit generates M02T-P, the set input of flip-flop FF2 is enabled. After DL3 delays the high output of DRl 45 nsec, 13 inverts the high output of DLl (45) which disables G4 and triggers and sets FF2. As a result, CKFS-P (waveform N, figure 28) is generated and routed to the CPU control circuit and CPU register file circuit.

5-291. After DL3 delays the high output of DR1 60 nsec, I7 inverts the high output of DL3 (60) which removes C60A-P (waveform I, figure 28). The **low** output of I7 disables G3 and resets FF3 which removes CKTS-P (waveform K, figure 28) and CKTR-N (waveform L, figure 28).

5-292. After DL3 delays the high output of DRl 75 nsec, I4 inverts the high output of DL3 (75) which removes CKDO-P (waveform J, figure 28). The low output of I4 resets FF2 which removes CKFS-P (waveform N, figure 28). After the low output of DRl is delayed 150 nsec, DL3 generates Z150-N (waveform O, figure 28) which is routed to the CPU address recognition circuit. After the high output DRl is delayed 150 nsec, DL3 removes Z150-P (waveform 0, figure 28).

5-293. When the CPU is in the halt mode and is addressed to perform an operation, the CPU address recognition circuit generates CKEN-P (waveform A, figure 28). CKEN-P activates gate Gl which triggers and sets FFl. Also, if the CPU ALU circuit is to perform logical operations rather than arithmetic operations, the CPU microcode register circuit generates M32T-P which enables G4. The 1 output of FFl activates G2 and the CPU central timing control circuit cycles as explained previously, Also, if data is to be written into a register in the CPU register file circuit, the CPU microcode register circuit generates M02T-P which enables the set input of FF2. FF2 then generates CKFS-P as explained previously.

5-294. When the CPU is in the halt mode and is addressed to perform an operation, the CPU address recognition circuit generates CKEN-P (waveform P, figure 28). Also, if an arithmetic operation is to be performed by the CPU ALU circuit, M32T-P is not generated which disables G4. CKEN-P activates Gl which triggers and sets FFl. The 1 output of FFl activates G2 and G5. The output of G5, CKOO-P (waveform Q, figure 28), is routed to the CPU control circuit. The output of G2 is coupled through DRl and the low output of DRl, CKME-P (waveform R, figure 28), is routed to DL3 and the CPU microcode register circuit. I8 inverts CKME-P which resets FF4 and generates CMEN-N (waveform S, figure 28) which is routed to the CPU address recognition circuit. CMEN-N also disables G5 which removes CKOO-P (waveform Q, figure 28). The pulse width of CKOO-P is determined by the inherent delays of G2, DRl, I5, and I8.

5-295. After DL3 delays the low output of DR1 15 nsec, I2 inverts the low output of

DL3 (15) generating CKML-P (waveform T, figure 28) which is routed to the CPU microcode register circuit. CKML-P also enables G6 and G7. After DL3 delays the low output of DRl 30 nsec, I6 inverts the low output of DL3 (30) generating CKRD-P (waveform U, figure 28) which is routed to the CPU control circuit and CPU register file circuit. CKRD-P also activates G6 which generates XSET-N (waveform V, figure 28). XSET-N is routed to the CPU register file circuit.

5-296. After DL3 delays the low output of DRl 45 nsec, I3 inverts the low output of DL3 (45). The output of I3 is inverted by inverter I1 which disables Gl. After DL3 delays the low output of DRl 60 nsec, I7 inverts the low output of DL3 (60) and generating C60A-P (waveform W, figure 28) which is routed to the CPU control circuit. C60A-P also activates G3 which resets FFl and disables G2. The 1 output of FFl disables G2 and G5.

5-297. The high output of G2 is coupled through DRl and the high output of DRl is inverted by 15 which removes CKME-P (waveform R, figure 28). The low output of 15 is inverted by I8 which removes CMEN-N (waveform S, figure 28). After DL3 delays the high output of DRl 15 nsec, 12 removes CKML-P (waveform T, figure 28) which disables G6 and triggers and sets FF3. Disabling G6 removes XSET-N. FF3 generates CKTS-P (waveform Y, figure 28) and CKTR-N (waveform Z, figure 28) which are routed to the CPU control circuit.

5-298. After DL3 delays the low output of DRl 75 nsec, I4 inverts the low output of DL3 (75) generating CKD0-P (waveform X, figure 28) which is routed to the CPU control circuit. After DL3 delays the high output of DRl 30 nsec, I6 inverts the high output of DL3 (30) and removes CKRD-P (waveform U, figure 28) which disables G6 and triggers and sets FF4. Setting FF4 generates CKSR-N (waveform AA, figure 28) which is routed to the CPU sequence register and microcode storage circuits.

5-299. After DL3 delays the low output of DRl 90 nsec, G3 is disabled and its output enables G2. After DL3 delays the high output of DRl 45 nsec, I3 inverts the high output of DL3 (45) which triggers and sets FF2. FF2 generates CKFS-P (waveform BB, figure 28) which is routed to the CPU control circuit and CPU register file circuit. The output of I3 is also inverted by I1 which enables Gl (end of cycle).

5-300. After DL3 delays the high output of DRl 60 nsec, I7 inverts the high output of DL3 (60) removing C60A-P (waveform W, figure 28) which resets FF3. With FF3 reset, CKTS-P (waveform Y, figure 28) and CKTR-N (waveform Z, figure 28) are removed. After DL3 delays the high output of DR1 75 nsec, I4 removes CKDO-P (waveform X, figure 28) which resets FF2. With FF2 reset, CKFS-P (waveform BB, figure 28) is removed. After DL3 delays the low output of DRl 150 nsec, DL3 generates Zl50-N (waveform CC, figure 28) which is routed to the CPU address recognition circuit. After DL3 delays the high output of DRl 150 nsec, DL3 removes Z150-N (waveform C, figure 28).

5-301. When the CPU is in the run mode, the CPU address recognition circuit continuously generates CKEN-P. Each time G1 is enabled, CKEN-P will activate Gl which causes the CPU central timing circuit to continuously cycle for as long as CKEN-P is being generated by the CPU address recognition circuit.

5-302. CORE MEMORY CONTROLLER AlA3A8 COMMAND AND PAGE SELECT CIRCUIT.

5-303. General. The Core Memory Controller command and page select circuit controls the transfer of data between the Core Memory and INFIBUS. It also controls transfers of data into selected pages of Core Memory on assigned addresses. The pages are first selected and stored by the Core Memory Controller command and page select circuit. When the Core Memory Controller command and page select circuit receives any of the assigned page addresses (C000 16 through DFFF 16), data is transferred into or out of the selected page. One of sixteen pages may be selected and they all use the same assigned page addresses with the variable being the stored selected page number which is used to modify the address of each page.

5-304. Detail Analysis (see figure 29). The Core Memory full cycle input, FULL CYC-P, and the memory select input, MEM SEL-F, are always generated (tied to 5 volts) which causes the Core Memory to always be selected and perform only full cycle operations. The Core Memory read only input, RD ONLY-P, is always disabled (tied to ground) which prevents the Core Memory from performing a read only operation.

5-305. Initially, the Core Memory Controller is cleared by master reset pulse, MRES-N. MRES-N is inverted by inverter I19 and the output of I19 is inverted by inverter I20. The low output of I20 clears the page register U57 an-l flip-flops FF4 and FF5. When the Core Memory is not being accessed, the memory available input, MEM AVAIL-P, from Core Memory is high, enabling gate G3 and single shot SS2. The strobe input, STRB-N, is normally high and inverted by inverter I3 which resets the command register U35 and the read/write register U50. The output of I3 also presets flip-flop FF2 and disables gate G21. The Ql output of the read/write register U50 is low which resets flip-flop FFl and the Q3 output is low which resets flip-flop FF3. The 0 output of FF2 disables gates G10 and G11. The output of gate Gl is high for all addresses except addresses between E000 and FFFF and the high output is routed to the Dl input of the command register U35.

5-306. If a master function is writing a 16-bit data word into the Core Memory, it places a Core Memory address on the INFIBUS address lines, data on the INFIBUS data lines, and generates RITE-N for a write operation. The INFIBUS address is modified and transferred to the Core Memory address input lines by the Core Memory Controller address transfer circuit. The data is transferred to the Core Memroy data input lines by the Core Memory Controller data transfer circuit.

5-307. RITE-N (waveform A, figure 3(j) is inverted by inverter I5 and the high output is routed to the D3 input of the read/write register U50. Inverter a also inverts the high output of Is, placing a low on the D1 input of read/write register U50. The master function then generates its strobe, STRB-N (waveform B, figure 30), which is inverted by I3. The output of I3 triggers single-shot SSl and enables gate G21. 40 nsec later, SSl resets and its output triggers command register U35 and FF2.

5-308. At this time, command register U35 is loaded with the high Dl input and the Ql output enables gate G5 and activates G3. The output of G3 is inverted by inverter I7 which activates gate G4 triggering read/write register U50. The Q1 output of command register U05 is low which activates gate G23 and its output enables gate G22. The Q3 output of command register U35 is low and is inverted by inverter I2 and its output, BYTE MODE-N, is high which activates gates G13 and G16. The output of G13 enables gate G14 and the output of G16 enables G17. Command register U35 Q3 output is high which is inverted by I4 and the output of I4 BYTE MODE-P is low. With BYTE MODE-N high and BYTE MODE-P low, the Core Memory Controller data transfer circuit selects the full 16-bit data word to be transferred to the Core Memory.

5-309. With RITE-IN low, read/write register U50 is loaded with a high D3 and D4 input. The Q3 output of read/write register U50 is high which enables FF3 to be set. The Q3 output of read/write register U50 is low which activates SS2 and the Q4 output is high which activates G4 until read/write register U50 is cleared.

5-310. SS2 remains set for 250 nsec. The 1 output of SS2 is high which activates G14 and G17. The outputs of G14 and G17 are coupled through drivers DRl and DR2, respectively, generating ZWl-P (waveform C, figure 30) and ZW2-P (waveform D, figure 30). ZWl-P (right byte) and ZW2-P (left byte) commands the Core Memory to accept both zones (9-bits/zone). The 0 output of SS2 is low which is inverted by inverter I13. The high output of I13 is coupled through driver DR3 which generates WT INIT-P (waveform E, figure 30). WT INIT-P commands the Core Memory to initiate a write cycle for the incoming word. After a delay, MEM AVAIL-P (waveform F, figure 30) goes low indicating the Core Memory is busy.

5-311. After 250 nsec, SS2 resets and the 0 output goes high, triggering and setting FF3. The 0 output of FF3 activates gate G20 which activates G21. Inverter I14 inverts the output of G20 and its output is delayed by DLl for 50 nsec. Inverter I15 inverts the output of G21 and its output is delayed by DL2 for 50 nsec. After the delay of DLl, G21 is disabled and after the delay of DL2, G22 is activated. The low output of G21 is inverted by I15 and the high output of I15 is again delayed by DL2 for 50 nsec. Therefore, G22 is activated for 50 nsec generating DONE-N (waveform G, figure 30).

5-312. The DONE-N output indicates to the master function a completed data transfer. The Core Memory Controller is then reset to the initial condition once again as explained previously (STRB-N is removed). The Core Memory normally cycles in 750 nsec, writing the word in the addressed location, and then generates MEM AVAIL-P once again, enabling the next Core Memory cycle to occur.

5-313. If the data to be transferred is an 8-bit byte, the master function would also generate BYTE-N, and the address bit ABOO-P, being high or low, will determine which zone the Core Memory will write the byte into. Inverter I1 inverts BYTE-N presenting a high D3 input to command register U35. Also, if the byte is to be written in zone 1, ABOO-P is high presenting a high D4 input to command register U35. If the byte is to be written into zone 2, ABOO-P is low, presenting a low D4 input to command register U35. When command register U35 is loaded (triggered by SS1), the Q3 output is high which is inverted by I2 generating BYTE MODE-K. Also Q3 is low which is inverted by I4 generating BYTE MODE-P.

5-314. If ABOO-P is high, the Q4 output of command register U35 will be high which activates G13. The output of G13 enables G14. When SS2 is triggered, as explained previously, G14 is activated. The output of G14 is coupled through DRl generating ZWl-P (zone 1). If ABOO-P is low, the Q4 output of the command register is high which activates G16. When SS2 is triggered, as explained previously, G17 is activated. The output of G17 is coupled through DR2 generating zw2-P (zone 2).

5-315. If a read operation of a 16-bit word is requested by a master function, the master function presents an address on the INFIBUS address lines and RITE-N (waveform A, figure 31) will remain high. 15 inverts the high RITE-N input and presents a low D3 input to read/write register U5O. The output of 15 is also inverted by 16 which presents a high Dl input to read/write register U50.

5-316. The r-aster function now generates its strobe, STRB-N (waveform B, figure 31). I3 inverts STRB-N which triggers SSl and also enables G21. After 40 nsec, SSl resets which triggers command register U35, loading it with the high Dl input. The Q1 output goes low which activates G23. The output of G23 enables G22. The Ql output goes high which enables G5 and activates G3. The output of C3 is inverted by I7 which activates G4. The output of G4 triggers read/write register U50 and loads it with the high Dl input (RITE-N high). At the same time, command register U35 Q3 output is low which is inverted by I2. The output of I2 enables gate G12, and the Q3 output is high which is inverted by I4. The output of I4 activates gate G18. The output of G18 enables gate G19. When read/write register U50 is triggered, the Ql output goes high which enables FFl to be set and the Q1 output goes low which triggers single-shot SS3. SS3 remains set for 250 nsec, and the output is coupled through driver DR4 which generates RD INIT-P (waveform C, figure 31). RD INIT-P commands the Core Memory to initiate a read cycle.

5-317. The Core Memory performs a read cycle within 300 nsec, presenting data to the Core Memory Controller data transfer circuit and generating DATA AVAIL-N (waveform D, figure 31) to indicate data is available. DATA AVAIL-n' is inverted by inverter I8 which sets FFl. The 1 output of FFl activates G5 which **activates** G12 and G19 generating DAEN-P (waveform E, figure 31) and DBEN-P (waveform F, figure 31) respectively, which are routed to the Core

Memory Controller data transfer circuit. The data from the Core Memory is then placed on the INFIBUS data lines. The 0 output of FF1 activates G20 generating DONE-N (waveform G, figure 31), as explained previously. After a delay, the master function releases the INFIBUS and the Core Memory Controller is cleared as explained previously.
the data read from the Core Memory is from zone 1 or zone 2. For zone 1, ABOO-P is high at the D4 input of command register U35. When command register U35 is triggered, it will be loaded with high D3 and D4 inputs. The Q3 output of command register U35 is inverted by I2 which disables G12. The 3 output of command register U35 is low and inverted by I4 which enables gate G15. The Q4 output of command register U35 is low and it activates G18 which enables G19. When G5 is activated as explained previously, only G19 is activated which generates DBEN-P. DBEN-P is routed to the Core Memory Controller data transfer circuit which causes the zone 1 data from the Core Memory to be placed on the INFIBUS data lines (DBOO-N through DB07-N).

5-318. For reading data out of the Core Memory in bytes operation is similar to when a word is to be read from the Core Memory, except the master function will also generate BYTE-N. I1 inverts BYTE-N and presents a high at the D3 input of the command register U35. Address bit ABOO-P will determine if

5-319. Operation during a zone 2 read cycle is similar to a zone 1 read cycle, except the data stored in zone 2 of the selected address in the Core Memory is placed on the INFIBUS data lines. When a zone 2 read cycle is requested, ABOO-P is low and the Q4 output of command register U35 will be high which enables G15 (G15 will also be enabled by the output of 14). When G5 is activated, as explained previously, only G15 is activated, generating DCEN-P which is routed to the Core Memory Controller data transfer circuit. DCEN-P causes the zone 2 data read from the Core Memory to be strobed to the zone one bit positions of the INFIBUS data lines (DBOO-N through DB07-N).

5-320. To transfer data into or out of the Core Memory pages, the Core Memory Controller must be set at the page where transfers are to be done. Under control of the stored software program, the master function generates address FFFF l6 on the INFIBUS address lines and the number of the page, 0000 16 to OOOF 1_6 on the INFIBUS data lines with RITE-N low. The Core Memory Controller address transfer circuit generates ABOO-P through AB15-P. Gates G6, G7 and G9 are activated by AB00-P through AB11-P and their outputs are inverted by inverters I10, Ill and I12 which enables gate G8. AB15-P enables the page command decoder U34 and with ABl2-P through AB14-P high, the Y7 output is low. Gate GI is activated and inverter I9 inverts the low Y7 output which activates G8. RITE-N is inverted by I5 which enables gate G11. The page number, DBOO-P through DB03-P, from the Core Memory Controller data transfer circuit is routed to the Dl through D4 inputs of page register U57.

5-321. The master function now generates its strobe, STRB-N, which is inverted by I3. The output of I13 triggers SSl and enables G21. In 40 nsec SSl resets which clears FF2. The 1 output of FF2 (low) activates G23 which enables G22 and the 0 output of FF2 (high) activates G11. The output of G11 is inverted by inverter I18, generating lF6-1 which triggers page register U57, loading it with the binary coded page number. Gate G24 is also activated by the output of G11 which activates G20, generating DONE-N.

5-322. The outputs of page register U57 represent the page number and activate or disable gates G46 and G48. PO-N through P3-N (page number code) are routed to the Core Memory Controller data transfer circuit. PO-P, Pl-N, IHO6-P, and IJ17-P are routed to the Core Memory Controller address transfer circuit where they are used to modify the page addresses (CO00 1_6 through DFFF $_{i6}$) of the selected page. The same range of INFIBUS addresses is used for each page but the addresses are modified for each page. Page register U57 stores the selected

page number until another page is selected or system reset, MRES-N, is initiated.

5-323. Deleted.

5-324. Once a page is selected and stored in page register U57, addresses COO0 16 through DFFF l6 are used to read from or write into the selected page. The cycles of reading or writing words or bytes into the Core Memory pages are similar to the read and write cycles explained previously except: for addresses COO0 16 through CFFF l6, AB15-P will be high which will enable page command decoder U34 and AB14-P is high which causes the Y4 output of page command decoder U34 to go low for this range of addresses. For addresses DO00 16 through DFFF l6, AB15-P is high enabling page command decoder U34. AB14-P and AB12-P are high and the Y5 output of page command decoder U34 is low. In both ranges of these addresses G2 is activated providing a high D2 input to command register U35. Gl is disabled for these ranges of addresses. If the address exceeds $DFFF_{16}$, the Y6 or Y7 output of page command decoder U34 will go low which activates Gl, providing a low Dl input to command register U35. The Ql output of command register U35 will be low and G3 and G5 will be disabled which prevents the Core Memory Controller from transferring data to or from Core Memory.

5-325. When command register U35 is loaded with a high D2 input (page mode), as explained previously, the Q2 output of command register U35, PAGE MODE-P, will go high, **and** the Q2 output of command register U35, PAGE MODE-N, will go low, PAGE MODE-P and PAGE MODE-N are routed to the Core Memory Controller address transfer circuit where they enable the stored page number (PO-P, Pl-N, IH06-P, and IJ17-P) to modify the incoming address to the Core Memory. The remainder of the cycle will be identical to a read or write cycle as explained previously.

5-326. When writing a 16-bit data word into the Core Memory, the Core Memory Controller data transfer circuit will transfer the data' to the Core Memory and also generate DBOO-P through DB15-P inputs. DBOO-P through DB07-P are routed to the exclusive-or gates G30, G32, G33, and G38 and DB08-P through DB15-P are routed to exclusive-or gates G39, G43, G44, and G47. The outputs of these gates are routed to the inputs of exclusive-or gates G31, G34, G40, and G45 and their outputs are routed to exclusive-or gates G35 and G41. The data bits (DBOO-P through DB15-P) will have logic levels determined by the data to be transferred and the exclusive-or gates will be activated or disabled according to these levels. The outputs of G35 and G41, PLO-P and PHI-P are the parity bits which are routed out to the Core Memory Controller data transfer circuit to be placed on the data lines with the data word to be transferred to the Core Memory. PLO-P is placed on the 8-bit data line and PHI-P is placed on the 17-bit data line for word transfers. During byte transfers, only DBOO-P through DB07-P are generated by the Core Memory Controller data transfer circuit. Only the output of G35, PLO-P, will be used with the byte of data transferred to the Core Memory. When the byte of data is placed in zone 1 of the Core Memory, PLO-P is placed on the 8-bit data line to the Core Memory. When the byte data is placed in zone 2 of the Core Memory, PLO-P is placed on the 17-bit data line to the Core Memory.

5-327. When the data word is written into the Core Memory, the parity bits (PLO-P and PHI-P) are also written with the data word. When the same word is read out of the Core Memory, the output of I2 BYTE MODE-N is high enabling gate G26 and the output of

G19, DBEN-P, is high enabling gate G29. The Ql output of read/write register U50, R/R-P, is high which enables gate G25 . The Core Memory presents the data word to the Core Memory Controller data transfer circuits and will be strobed to the INFIBUS. The Core Memory Controller data transfer circuit generates the same DBOO-P through DBl5S-P combination of data bits to the exclusive-or gates G30, G32, G33, G38, G39, G43, G44, and G47. If there was no error in transferring the data between Core Memory and Core Memory Controller (loss of bits or noise injected hits), the same combination of exclusive-or gates will be disabled or enabled which causes PLO-P and PHI-P to assume the same logic levels as when the data was written into the Core Memory. At the same time, the Core Memory generates the parity bits, D008-P and D017-P, which will have the same levels as PLO-P and PHI-P. D008-P and D017-P will activate or disable G26 or G29 which activates or disables G28. If the output of G35 is the same level as the output of G28, exclusive-or gate G36 will be disabled which presents a low to the set input of flip-flop FF4.

5-328. When DONE-N is generated, inverter I16 inverts DONE-N and generates DONE-P which activates G25. When DONE-N is removed, DONE-P is also removed which disables G25. The low-to-high output of G25 triggers FF4 which remains cleared. If there was a bit position of the data in error, the output of G35 will be different from DOO8-P. The high and low inputs to G36 will activate it, presenting a high to the set input of FF4 when FF4 is triggered, it will set. The 0 output of FF4 will activate G37 which generates PARERP-P. The exclusive-or gate G42 with the outputs of G26 and G41 operates in the same manner to set flip-flop FF5 when an error is detected in the word read out of Core Memory.

5-329. During byte data transfers the error logic operates in a manner similar to word transfers, except when data is read out of zone 2 of Core Memory, DCEN-P enables gate G27 for the PI-II-P parity bit (stored in D017-P position) to activate or disable G27 when data is read out. When reading zone 1, DBEN-P enables G29 for the PLO-P parity bit (stored in D008-P position) to activate or disable G29. If an error exists in zone 1 or 2, FF4 will be set as explained previously.

5-330. CORE MEMORY CONTROLLER AlA3A8 ADDRESS TRANSFER CIRCUIT.

5-331. General. The Core Memory Controller address transfer circuit converts INFIBUS address to Core Memory address and transmits them to the Core Memory.

5-332. Detail Analysis (see figure 31). Inverter I1 and associated address receivers invert the address bits, ABOO-N through AB15-N, from the INFIBUS address lines and generates ABOO-P through AR15-P. Address data ABOO-P through AB15-P are routed to the Core Memory Controller command and page select circuit, the address selector/driver gates and the address drivers. The Core Memory Controller command and page select circuit decodes the addresses and determines whether or not the address is a low order address or page address.

5-333. When a low order Core Memory address is received, PAGE MODE-P from the Core Memory Controller command and page select circuit is low and PAGE MODE-N is high. Driver DRl and associated address drivers will couple ABOl -P through AB12-P to the Core Memory input address lines, AIOO-P through AI11-P. With PAGE MODE-P low G2 is disabled which causes AI15-P to remain low for all low order addresses. PAGE MODE-P (low) will also enable the associated address selector/driver gates to couple AB13-P through ABl5-P to Core Memory input address lines, AI12-P through AI14-P.

5-334. When a page address is received, the address is first modified then transferred. The Core Memory Controller command and page select circuit generates PAGE MODE-P, PAGE MC3E-N and a combination of PO-P, Pl-P, IJ17-P and IH06-P which is the page number. ABOl-P through AB12-P are coupled through the address drivers as explained previously. AB13-P through AB15-P are blocked (PAGE

MODE-P activates G2 and associated gates). PAGE MODE-N enables gate Gl and associated address selector/driver gates to couple PO-P, Pl-N, IJ17-P and IH06-P (page number) to the Core Memory input address lines, AI12-P through AI15-P, respectively.

5-335. CORE MEMORY CONTROLLER AlA3A8 DATA TRANSFER CIRCUIT.

5-336. General. The Core Memory Controller data transfer circuit receives and transmits data to and from the INFIBUS data lines and Core Memory under control of the Core Memory 'Controller command and page select circuit.

5-337. Detail Analysis (see figure 33). The data bus driver/receivers (inverters I2 and I3) receive the data word, DBOO-N through DB15-N, from the INFIBUS and generates DBOO-P through DBl5-P. DBOO-P through DB15-P are routed to the Core Memory Controller command and page select circuits, and also to the data selector/drivers and the data drivers. The data selector/drivers and data drivers couple the data DBOO-P through DB15-P, and parity bits, PHI-P and PLO-P, to the Core Memory input data lines, DI08-P through DI17-P.

5-338. When data is to be transferred into the Core Memory (write) as a 16-bit word, the Core Memory Controller command and page select circuit generates both parity bits, PHI-P and PLO-P. Also, BYTE MODE-P is low and BYTE MODE-N is high. The low BYTE MODE-P enables gate G3 and associated data selector/drivers to couple DB08-P through DBl5-P and PHI-P to the Core Memory input data lines, DI09 -P through DIl7-P, respectively. Driver DRl and associated data drivers couple DBOO-P through DB07-P and PLO-P to the Core Memory input data lines, DIOO-P through CIO8-P, respectively.

5-339. When the data is to be transferred into the Core Memory (write) as an 8-bit byte, the data on the INFIBUS is right byte justified. That is, only DBOO-N through DB07-N will be received from the INFIBUS and only DBOO-P through DB07-P will be presented to the data selector/drivers and data drivers. The Core Memory Controller command and page select circuit generates the PLI-P parity bit, BYTE MODE-P and BYTE MODE-N. BYTE MODE-N enables gate G4 and associated data selector/drivers to couple DBOO-P through DB07-P and PLO-P to the Core Memory input data lines, DI09-P through DI17-P, respectively. Also, DRl and associated data drivers couple DBOO-P through DB07-P and PLO-P to the Core Memory input data lines, DI00-P through DI08-P, respectively. The data the Core Memory will accept, DIOO-P through DI08-P (zone 1) or DI09-P through DI17-P (zone 2), depends on the commands from the Core Memory Controller command and page select circuit to the Core Memory.

5-340. Data receivers (I1 shown) receive data from the Core Memory that is to be placed on the INFIBUS data lines. Inverter I1 and associated data receivers invert D000-P through D007-P and D009-P through D016-P, generating D000-N through D070-N and D090-N through D160-N, respectively.

5-341. When reading a 16-bit word out of the Core Memory, the Core Memory Controller command and page select circuit generates DAEN-P and DBEN-P. DBEN-P activates gate G2 and associated date bus driver/receivers coupling D000-N through DO70-N to the INFIBUS data lines, DBOO-N through DB07-N. Also, DAEN-P activates gate G1 and associated data bus driver/receivers coupling D090-N through D160-N to the INFIBUS data lines, DB08-N through DB15-N-

5-342. When reading data out of the Core Memory in 8-bit bytes, the Core Memory Controller command and page select circuit generaces DBEN-P for a zone 1 read or DCEN-P for a zone 2 read (determined by the address). DBEN-P, zone 1, activates G2 and associated data bus driver/receivers coupling D000-N through DO70-N to the INFIBUS data lines, DB00-N through DB07-N. DCEN-P, zone 2, activates gate G6 and associated data bus drivers coupling D090-N through D160-N to the INFIBUS data lines, DB00-N through DB07-N.

5-343. When the page number is to be read out of the Core Memory Controller,

PO-N through P3-N, which represents the page number, are routed to bus driver receivers U44 (G3 shown typical). RDST-P is generated which strobes the page number to the INFIBUS data lines, DBOO-N through DB03-N.

5-344. AUTOLOAD AlA3A9 CONTROL CIRCUIT.

5-345. General. The Autoload control circuit detects the autoload signal and causes the Autoload INFIBUS access circuit to generate a direct data transfer. When the direct data transfer is complete, the Autoload control circuit then causes the Autoload INFIBUS access circuit to generate a level 1 interrupt request for data transfer. When the Autoload address recognition and ROM select circuit recognizes the Autoload address, the Autoload control circuit clocks and controls the Autoload ROM and data select circuit.

5-346. Detail Analysis (see figure 34). Initially, the Autoload control circuit receives a master reset pulse, MRES-N from the INFIBUS. MRES-N is inverted by inserter I2 and the output of I2 is inverted by inverter I3. The output of I3 resets flip-flops FF2 and FF6, resets the S-bit shift register U65, and activates gates G5 and G6. The output of G5 resets flip-flop FF3 and the output of G6 resets flip-flop FF4. The output of I2 is also inverted by inverter I1 which resets flip-flop FF1 and single shots SSl and SS2. Also, AMAS-P is normally low holding flip-flops FF5 and FF7 reset.

5-347. When an Autoload pulse, ATLD-N, is generated by the Program Maintenance Pans: or Bus Controller, it is coupled through driver DRl which activates gate Gl. The trailing edge of the Gl output sets FF1 which will remain set until the next MRES-N pulse is received. The output of FF1 triggers SSl. The 0 output of SSl activates gate G4 which resets flip-flops FF8 and FF9. 140 msec late: the trailing edge of the 1 output of SSl triggers FF2 which disables Gl. The 0 output of FF2 sets FF3 and RLDS-P and RLDR-N are generated. With RLDS-P high and RLDR-N low, a direct data transfer INFIBUS access is requested by the Autoload INFIBUS access logic circuit and, when gained, 0006 16 is strobed to the INFIBUS address lines and the address FBOO is strobed to the INFIBUS data lines. When the direct data transfer is complete, DONE-N goes low for 50 nsec. DONE-N is inverted by inverter I8. The output of I8, BDNA-P, causes the Autoload INFIBUS access circuit to cause ACLK-N to go low for 50 nsec. ACLK-N activates G5 which resets FF3. The output of I8 is also inverted by inverter I7 which presets FF6. Presetting FF6 insures FF2 will not be set until after another MRES-N pulse is received. Resettling FF3 sets FF4 which causes the Autoload INFIBUS access circuit to generate a level 1 interrupt data transfer request. When the level 1 interrupt data transfer is complete BOLK-N goes low for 50 nsec activating G6 which resets FF4.

5-348. If the Autoload control circuit does not receive a DONE-N pulse within 2 usec after INFIBUS access is gained, ABRT-N goes low, activating G5 and G6 which resets FF3 or FF4 depending on which one was set.

5-349. The 25 MHz clock pulses, CLKA-N (waveform A, figure 35), are coupled through inverter I10 and divided by two by flip-flop FFl0. Gate G8 is enabled by the 5 volts and gate G10 is disabled by the logic 0 out of inverter I9. The 12.5 MHz pulses out of FF10 activates G8 which activates gate G9 at a 12.5 MHz cate. If the J4 jumper was installed, G10 would be activated and G8 would be disabled. The 12.5 MHz output of FF 10 would be divided by two by flip-flop FF11. This 6.2.5 MHz output of FF11 would activate G10 which would activate G9 at a 6.25 MHz rate.

5-350. The 12.5 MHz output of G9 waveform B, figure 35) enables gates G11 and G12 at a 12.5 MHz rate and is divided by two by flip-flop FF12. The 1 output of FF12 enables G11 at a 6.25 MHz rate and the 0 output of FF12 acti-

vates G12 at a 6.25 MHz rate. The output of G12 is inverted by inverter I11. The output of I11, STAB-P (waveform figure 35), enables gate G2 at a 6.25 MHz rate and clocks the Autoload ROM and data circuit.

5-351. When the Autoload address recognition and ROM select circuit recognizes the Autoload address on the INFIBUS address lines, AMAS-P goes high and AMAR-N goes low for the duration of STRB-N. When AMAS-P is high, FF5 and FF7 are enabled to be set. When AMAR-N (waveform D, figure 35) goes low, SS2 is triggered and the 80 nsec positive pulse out of SS2 is routed to and sets the first stage of the S-bit shift register U65. The trailing edge of the SS2 output sets FF8. The next negative going edge out of G9, after FF8 sets, sets FF9 (waveform E, figure 35) which activates G11. The output of G11 (waveform F, figure 35) triggers the S-bit shift register U65 five times generating STA2-P (waveform G, figure 35), STA3-P (waveform H, figure 35), STA4-P (waveform I, figure 35), and STA5-P (waveform J, figure 35). STA5-P enables gate G2 to be activated by STAB-P. The output of G2, SSRM-P (waveform K, figure 35) is routed to the Autoload ROM and data circuit. The trailing edge of the output of G2 sets FF5 causing SRDS-P to go high. The output of FF5 is inverted by inverter I4, delayed 50 nsec by DL2 and then inverted by inverter I5. Also, when AMAR-N goes low, gate G7 is activated which enables gate G3. The output of I5 is inverted by inverter I6 and activates G3. The output of I6 is delayed 50 nsec by delay DL3 which disables G3 50 nsec after it was activated. The output of G3 is coupled through driver DR2 and onto the INFIBUS as DONE-N. The output of DR2 is also inverted by I8. The output of I8, BDNA-P is routed to the Autoload INFIBUS access logic circuit and inverted by I7 to ensure FF6 is preset.

5-352. The negative going edge of A1H5-P sets FF7 which activates G4. output of G4 resets FF8 and FF9. DONE-N causes STRB-N (Autoload INFIBUS access logic circuits) to go high which causes AMAS-P to go low and AMAR-N to go high. When AMAS-P goes low FF5 and FF7 are reset. The Autoload INFIBUS access circuit generates BCLK-N in response to BDNA-P. When BCLK-N goes low, G6 is activated which resets FF4.

5-353. If DONE-N is not received or generated within 2 usec after STRB-N goes low, QUIT-N (Autoload INFIBUS access logic circuit) causes ABRT-N to go low which activates G5 and G6. The output of G5 resets FF3 and the output of G6 resets FF4.

5-354. AUTOLOAD AlA3A9 ADDRESS RECOGNITION AND ROM SELECT CIRCUIT.

5-355. General. The Autoload address recognition and ROM select circuit detects the Autoload address on the INFIBUS address lines (Autoload being slaved after level 1 interrupt request), generates signals to select the ROM in the Autoload ROM and data circuit, receives STRB-N from the INFIBUS and routes STRB-N to the INFIBUS.

5-356. Detail Analysis (see figure 36). Switches Sl and S2, inverters I12 and I13, and gates G8 through Gl5 determine the level of the ROM select signals ERM1-N through ERM4-N. Switches Sl and S2 are al-ways in the up position. This causes the outputs of I12 and I13 to activate G14 which enables G15. If Sl and S2 were both in the down position, G8 would be activated which would enable G9. If Sl was in the up position and S2 was in the down position, G10 would be activated which would enable G11. If Sl was in the down position and S2 was in the up position, G12 would be activated which would enable G13.

5-357. Address bits AB08-N through AB15-N are coupled through inverters I1 through I8. The outputs of I1 through I15 are routed to gates G1 through G5 and the outputs of I6 through I8 are routed

to gate G6. When AB08-N, AB09-N, and AB11 -N through AB15-N are low and AB10-N is high G1 through G5 are disabled and G6 is activated. This high level output of Gl through G6 is routed to the set input of flip-flop FFl. When STRB-N goes low, it is inverted by inverter I9 causing STRA-P to go high. The output of I9 is also coupled through driver DRl. This high output of DRl allows FFl to be set and is also coupled through driver DR2. The output of DR2 is inverted by inverter I10. This negative going edge out of I10 causes FF1 to set. When FFl sets AMAS-P and AMAR-N are generated which activates the Autoload control circuit. Also, when FFl sets, G15 is activated. The output of G15, ERM4-N, enables the ROM in the Autoload ROM and data circuits. ERMl-N through ERM3-N are not generated because switches Sl and S2 are always in the up position. When STRB-N returns to high, the output of DRl goes low which resets FFl.

5-358. When the Autoload INFIBUS access circuit requires STRB-N to be generated, ONLN-P goes high which enables gate G7. ONLN-P is also inverted by inverter I11 then delayed 50 nsec by DL7 which activates G7, causing STRB-N to go low 50 nsec after ONLN-P goes high. When ONLN-P goes low, G7 is disabled and STRB-N returns to high. The output of I11, GEST-N, is also routed to the Autoload control circuit.

5-359. AUTOLOAD AlA2A9 INFIBUS ACCESS CIRCUIT.

5-360. General. The Autoload INFIBUS access circuit, under control of the Autoload control circuit, causes a direct data transfer to take place which stobes the address 0006 16 onto the INFIBUS address lines. At the same time, the Autoload address FB00 is strobed to the INFIBUS data lines. After the direct data transfer, the Autoload control circuit causes the Autoload INFIBUS access Circuit to generate a level 1 interrupt which strobes onto the INFIBUS data lines. The Autoload INFIBUS access circuit also places and monitors various signals on the INFIBUS to ensure a proper data transfer occurs.

5-361. Detail Analysis (see figure 37). When the Autoload control circuit receives the master reset pulse, MRES-N, ARES-P goes high which is inverted by inverter I8. The output of I8 clears flip-flops FFl through FF4 and FF8 through FF11. The 1 output of FF3 resets flip-flop FF6. QUIT-N (normally high) is inverted by inverter I4 which presets FF5.

5-362. With FF2, FF3 and FF4 reset, gate G10 is activated which enables gate G1. If no other function is requesting a direct data transfer, SELD-N will be high, also enabling Gl. 140 msec after the Autoload signal is detected on the INFIBUS, RLDS-P (waveform A, figure 38) goes high, activating Gl which sets FFl. The 0 output of FFl ensures flip-flop FF7 is cleared. The 1 output of FFl activates gate G14. The output of G14 is coupled through driver DRl causing SRLD-N (waveform B, figure 38) to go low. The Bus Controller detects SRLD-N and causes SELD-N to go low which disables Gl and the BUS Controller generates the precedence pulse, PCDA-P. Disabling Gl enables qate G2 and activates gate G15 which disables gate G16. When the precedence pulse, PCDA-P (waveform C, figure 38), is received, G2 is activated which sets FF2. The 0 output of FF2 disables G10 which in turn disables Gl. In addition, the 0 output of FF2 disables G14 which causes SRLD-N to return to high, and disables gate G24. The output of G24 is inverted by inverter I7 which sets FF7. The output FF7 activates G37 which ensures FF11 is cleared. The output of FF7 also activates gate G13 which ensures FF4 is cleared. The 1 output of FF2 enables gate G3 and activates gates G5 and G19, The output of G19 activates gate G20. The output of G20 is coupled through driver DR2 causing SACK-N (waveform

D, figure 38) to go low. The output of G5 sets FF3 and activates gate G28 causing ONLN-N (waveform E, figure 38) to go low. The 0 output of FF3 disables G10 which disables Gl. The 1 output of FF3 enables gates G9, G11, G12, G23 and G25, enables FF6 to be preset, and activates gate G7. The output of G7 activates gate G8 causing AONL-N (waveform F, figure 38) to go low. AONL-N also activates G28, generating ONLN-P. When PDCA-P returns to low, G2 is disabled which activates G3. The output of G3 clears FFl which disables G2.

5-363. 50 nsec after ONLN-P goes high, STRA-P (waveform G, figure 38) goes high which activates G11 and enables gate G27. STRA-P is also inverted by inverter I2 which disables G5 (ONLN-P remains high because AONL-N still Pow). Activating G11 clears FF2. With AONL-N and ONLN-N low, the address 0006_{16} is strobed to the INFIBUS address lines and the Autoload address FB00 is strobed to the INFIBUS data lines.

5-364. When the direct data transfer is complete, the addressed function (Core Memory Controller) generates DONE-?! which causes the Autoload control circuit to generate BDNA-P (waveform H, figure 38). When BDNA-P goes high, G9 and G12 are activated. The output of G12, ACLK-N (waveform I, figure 38), sets FF4 and disables G7 and the output of G9 holds G8 activated. BDNA-P also activates G25 causing BEND-N to be generated. Setting FF4 enables gate G7. BDNA-P is also inverted by inverter I3. When BDNA-P returns to low, the output of I3 returns to high which activates G6. The output of G6 clears FF3, Clearing FF3 disables G7, G9, G11, and G12 causing ACLK-N and AONL-N to return to high. Clearing FF3 also activates gate G13 which clears FF4.

5-365. ACLK-N also causes INTS-P (waveform J, figure 38) from the Autoload control circuit to be generated. With FF8, FF9 and FF11 still cleared, gates G24, G26 and G37 are enabled and gate G29 is activated which enables gate G32. INTS-P activates G32 which sets FF10. The 0 output of FFlO clears FF7. The 1 output of FF10 enables gate G17 and G33 and activates G26. The output of G26 is coupled through driver DR3 which generates SRLl-N (waveform K, figure 38). In response to SRLl-N the Bus Controller causes SELl-N to go low which disables G32. The high output of G32 now enables G33 and activates G17 which disables G16. Also, the Bus Controller generates the precedence pulse a second time. When the precedence pulse, PCDA-P, goes high, G33 is activated which sets FF8. The 1 output of FF8 enables G30 and activates gates G21 and G31. The output of G21 activates G20. The output of G20 is coupled through DR2 causing SACK-N to go low a second time. The output of G31 sets FF9 and activates G28 which causes ONLN-P to go high a second time. The 0 output of FF9 disables G29 which disables G32. The 0 output of FF8 also disables G24 and G26. The output of G24 is inverted by I7 which sets FF7. Setting FF7 activates G37 which ensures FF11 is cleared. Disabling G26 causes SRLl-N to return to high. The 1 output of FF9 enables gates G22, G25, G27, G35, and G36. When PCDA-P returns to low, G33 is disabled which activates G30. The output of G30 clears FF10.

5-366. 50 nsec after ONLN-P goes high the second time, STRA-P goes high a second time activating G27 which clears FF8. The output of FF8 enables G26 and the 1 output of FF8 disables G21 which causes SACK-N to go high. The output of FF9 disables G24, G29, and G37. The 1 output of FF9 activates G35 which causes BONL-N (waveform L, figure 38) to go low which holds ONLN-P high Clearing FF8 also disables G31. With ONLN-N high and BONL-N low, the Mag Tape Unit No. is strobed to the INFIBUS data lines.

5-367. When the level 1 interrupt data transfer is complete DONE-N causes the Autoload control circuit to generate

BDNA-P a second time. This second BDNA-P pulse activates G25 generating BEND-N and activates G36. The output of G36, BCLK-N (waveform M, figure 38), sets FF11, and activates G35 which holds ONLN-P high and BONL-N low until BDNA-P returns to low. The 1 output of FF11 enables G34. When BDNA-P returns to low, the output of I3 returns to high which activates G34. The output of G34 clears FF9 which disables G35. Disabling G35 causes BONL-P to return to low and disables G28 causing ONLN-P to return to low. The 0 output of FF9 activates G37 which clears FF11.

5-368. If during a direct data transfer BDNA-P is not received within 2 usec after STRB-N is generated, the Bus Controller generates QUIT-N. QUIT-N is inverted by inverter I4 and because BDNA-P was not received FF3 is still set. When the output of I4 goes high G23 is activated which presets FF6 and disables gate G18. This high output of G18 is inverted by inverter I6 which causes ABRT-N to go low. The 0 output of FF6 clears FF2 and FF3. The 1 output of FF3 now disables G23 which enables G18 and resets FF6 which activates G28 causing ABRT-N to return to high. The output of 14 is also inverted by inverter 15 to disable G5 until FF2 is cleared.

5-369. If, during a level 1 interrupt data transfer, BDNA-P is not received within 2 usec after STRB-N is generated by the Bus Controller, QUIT-N is gen-era ted. QUIT-N is inverted by I4 and because BDNA-P was not received FF9 is still set, thereby enabling G22. When BQTA-P goes high, G22 is activated which disables G18 and resets FF5. The high output of G18 activates G25, causing BEND-N to go low. In addition, the output of G18 is inverted by I6 causing ABRT-N to go low. When BOTA-P returns to low G22 is disabled and FF5 IS preset which activates G18 causing ABRT-N to go high. When FF5 resets, FF8 and FF9 are cleared. The Output of I4 is also inverted by I5 which disables G31 until FF8 is cleared.

5-370. AUTOLOAD AlA3A9 ROM AND DATA CIRCUIT.

5-371. General. The Autoload ROM and data circuit strobes the Autoload address to the INFIBUS data lines during a direct data transfer, strobes the Autoload device number (address) to the INFIBUS data lines during a level 1 interrupt data transfer, or strobes the ROM nibbles data register information to the INFIBUS data lines in word or byte format when the Autoload is being slaved (addressed).

5-372. Detail Analysis (see figure 39). During a direct data transfer RLDS-P (waveform A, figure 38) is high and AONL-N goes low and the start address is placed on the DBOO-N through DBl5-N INFIBUS data lines. When RLDS-P is high, the 0 volt and 5 volt inputs to data multiplexes U59 and U69 are coupled to bus drivers U60 and U70. When AONL-N (waveform F, figure 38) goes low, gate G18 is activated which strobes data bus drivers U60 and U70 causing DB08-N, DBO9-N and DB11-N through DB15-N to go low and DB10-N to remain high. During a direct data transfer RLDR-N is also low and when ONLN-P (waveform E, figure 38) goes high the first time, ABOl-N and AB02-N, are strobed to the INFIBUS address lines, causing ABOl-N and AB02-N to go low for the duration of ONLN-P. This action strobes address 0006 16 onto the INFIBUS address lines. RITE-N is also generated at this time.

5-373. During a level 1 interrupt data transfer, INTS-P (waveform J, figure 38) is high and BONL-N goes low and the Mag Tape Unit number is placed on the DBOO-N through DB03-N INFIBUS data lines. When INTS-P is high the 5 volt inputs and the inputs determined by the positions of switches S3 and S4 are coupled through the data multiplexer U39 and routed to data bus driver U40. When BONL-N (waveform L, figure 38) goes low, gate G21 is activated which strobes data bus driver U40 causing DBOO-N and DBO4-N to remain high and DB02-N and DB03-N to go to the levels determined

by S3 and S4. When Mag Tape Unit No. 1 will be used to load the tape program, switches S3 and S4 are in the down position which causes DBOO-N through DB03-N to remain high when BONL-N goes low. When Mag Tape Unit No. 2 will be used to load the tape program S3 is in the down position and S4 is in the up position which causes YB00-N, DB02-N and DB03 -N to remain high and DBOl-N to go low when BONL-N goes low. During a level 1 interrupt data transfer RLDR-N is high and when ONLN-P goes high, ABOO-N and ABOl-N remain high.

5-374. When the Autoload function is being addressed, the selected ROM outputs are clocked into the ROM nibbles data register and then strobed to the INFIBUS data lines in word or byte format. The address bits AB03-N through AB07-N are coupled through inverters I1 through I5 and address bits ABOl-N and AB06-N are coupled through inverters of address bus driver receivers U20 (18 typical). AOlA-P through A07A-P are routed to ROM 4 which is enabled by ERM4-N from the Autoload address recognition and ROM select circuit.

5-375. When the Autoload address recognition and ROM select circuits recognize the Autoload address on the INFIBUS address lines, AMAS-P (waveform A, figure 40) goes high enabling gates G17 and G22. Also, RLDS-P and INTS-P are low, which allows nibble bits N100-N through N103-N, N200-N through N203-N and N400-N through N403-N to be coupled through the data multiplexers U69, U59 and U39. If a word (16-bits or four 4-bit nibbles) is to be strobed to the INFIBUS data lines, BYTE-N is high and is inverted by inverter I12. This low output of I12 disables gates G6, G7, G12 and G13 and is inverted by inverter I13. This high output of I13 enables gates G2, G4, G11, and G15.

5-376. When STA2-P (waveform B, figure 40) goes high, the outputs of gates G1 and G3 are low because STA3-P, STA4-P, and STA5-P are low. This causes the outputs of ROM4 to assume a pre-programmed value (nibble 1). STA2-P also enables gate G2 which is activated by STAB-P (waveform C, figure 40). The output of G2 clocks the outputs of ROM 4 in to the ROM nibbles data register U68. The N100-N through N103-N outputs of the ROM nibbles data register U68 are coupled through data multiplexer U69 to the data bus drivers U70.

5-377. When STA3-P (waveform D, figure 40) goes high, the output of inverter I9 goes low activating G3. The output of Gl is still low and the output of G3 is high (address bits ABOl-N through AB07-N remain unchanged), which causes the outputs of ROM 4 to assume a second pre-programmed value (nibble 2). STA3-P also enables G4 which is activated by STAB-P. The output of G4 clocks the outputs of ROM 4 into the ROM nibbles data register U68. The N200-N through N203-N outputs of the ROM nibbles data register U68 are coupled through data multiplexer U59 to the data bus drivers U60.

5-378. When STA4-P (waveform E, figure 40) goes high, the output of inverter 16 goes low activating G1. The output of G1 is high and the output of G3 returns to low because STA3-P has returned to low (address bit A301-N through AB07-N remain unchanged). The outputs of Gl and G3 now cause the outputs of ROM 4 to assume a third pre-programmed value (nibble 3). STA4-P also enables gate G10 which is activated by STAB-P. The output of G10 activates gate G11 which activates gate G8. The output of G8 clocks the outputs of ROM 4 into the ROM nibbles data register U48. The N300-N through N303-N outputs of ROM nibbles data register U48 are routed to the data bus drivers U50.

5-379. When STA5-P (waveform F, figure 40) goes high, the output of inverter I7 goes low activating Gl and G3 (address bits ABOl-N through AB07-N remain unchanged). The outputs of G1

and G3 (high) cause the outputs of ROM 4 to assume a fourth pre-programmed value (nibble 4). SSRM-P (waveform G, figure 40) activates G15 which activates gate G14. The output of G14 clocks the outputs of ROM 4 into the ROM nibbles data register U48. The N400-N through N404-N outputs of ROM nibbles data register U48 are coupled through data multiplexer U39 to data bus drivers U40.

5-380. When SSRM-P returns to low, SRDS-P (waveform N, figure 40) goes high. SRDS-P activates G17 and G22. The output of G17 activates G18 which strobes the outputs of the data multiplexers U59 and U69 through the data bus drivers U60 and U70 and onto the INFIBUS data lines DB08-N through DBl5-N. At the same time the output of G22 activates G21 and is inverted by inverter I14. The output of I14 strobes N300-N through N303-N through the data bus driver U50 and onto the INFIBUS data lines DB04-N through DB07-N. The output of G21 strobes the outputs of data multiplexer U39 through the data bus driver U40 and onto the INFIBUS data lines DBOO-N through DB03-N.

5-381. If the Autoload recognizes its address and a byte (8-bits or two 4-bit nibbles) is to be strobed to the INFIBUS data lines, BYTE-N is low and is inverted by I12. This high output of I12 enables G6, G7, G12, and G13 and is inverted by I13. This high output of I13 disables gates G2, G4, G11, G15 and G17. Also AMAS-P is high enabling G22,

5-382. If ABOO-N, is high the output of inverter I10 disables G6 and G12. The output of I10 is also Inverted by inverter Ill which enables G7 and G13. When STA2-P goes high nibble 1 (first pre-programmed value of the out put of ROM 4) is generated as explained previously. However, STA2-P now enables G7 which is activated by STAB-P. The output of G7 activates G8 which clocks nibble 1 into ROM nibbles data register U48. When STA3-P goes high nibble 2 (second pre-programmed **value** of the outputs of ROM 4) is generated as explained previously. However, STA3-P now enables G13 which is activated by STAB-P. The output of G13 activates G14 which clocks nibble 2 into ROM nibbles data register U48. No data is clocked into ROM nibbles **data** registers U48 and U68 during STA4-P and STA5-P because G2, G4, G6, G11, G12, G15 and G17 are disabled. When SRDS-P goes high N300-N through N303-N and N400-N through N403-N are strobed through data bus drivers U50 and U40 to the INFIBUS data lines DB07-N through DBOO-N, as explained previously.

5-383. If ABOO-N is low, the output of I10 enables G6 and G12 and the output of Ill disables G7 and G13. No data is clocked into the ROM nibbles data registers U48 and U68 during STA2-P and STA3-P because G2, G4, G7, G11, G13, G15 and G17 are disabled. When STA4-P goes high, nibble 3 (third pre-programmed value of the outputs of ROM 4) is generated, as explained previously. STA4-P enables G10 which is activated by STAB-P. The output of G10 now activates G6 which activates G8. The output of G8 now clocks nibble 3 into the ROM nibbles data register U48. When STA5-P is generated, nibble 4 (fourth pre-programmed value of the outputs of ROM 4) is generated as explained previously. When SSRM-P goes high, G12 is activated which activates G14. The output of G14 now clocks nibble 4 into ROM nibbles data register U68. When SRDS-P goes high N300-N through N303-N and N400-N through N403-N are strobed through data bus drivers U50 and U40 onto the INFIBUS data lines DB07-N through DBOO-N, as explained previously.

5-384. PARALLEL I/O AlA3A10 ADDRESS RECEIVERS AND RECOGNITION CIRCUIT.

5-385. General. The Parallel I/O address receivers and recognition circuit recognizes the Parallel I/O address when being slaved by a master function. It selects the internal registers of the Parallel I/O and performs a read or write operation as determined by the master function slaving the Parallel I/O.

5-386. Detail Analysis (see figure 41). The device number connector J3 connections determine the Parallel I/O address (device number). DN04-N through DN11-N, device number bits, are routed to the Parallel I/O data input and selector circuit to be placed on the INFIBUS data lines when the Parallel I/O is requesting a level 1 INFIBUS access. The device number inverters (14 shown) generate DA04-P through DA11-P. AB0l-N through AB15-N from the INFIBUS address lines are inverted by the address bus receivers U10, U20, U29, and U40 (11 shown) which generate A01A-P through Al5A-P.

5-387. A04A-P through A11A-P are applied to the address recognition exclusive-nor gates U19, U28, and U33 (Gl shown) where they are compared with the lumper encoded device number (DA04-P through DAll-P). If there is a match at the inputs, the corresponding outputs of address recognition exclusive-nor gates U19, U28, and U39 will be high. Also, for address recognition, A12A-P must be high which is coupled through driver DRl. In addition, A13A-P, A14A-P and A15A-P must be high which activates gate G2. The combined outputs of address recognition exclusive-nor gates U19, U28, and U39, driver DRl, and G2 will be high which places a high at the set input of flip-flop FF1.

5-388. Inverters I2, I3, and I5, and gates G3 through G6 decode A01A-P, A02A-P, and A03A-P to select the control, status, or data registers in the Parallel I/O data output and control register circuit. To select the control register, A01A-P and A02A-P are high and A03A-P is low. Gate G4 is enabled by A0lA-P and AO2A-P and the high output of I5. G4 is act!-vated and generates ACNT-N when FF1 is set. To select the status register, A0lA-P, A02A-P and A03A-F are all low and the high outputs of I2, I3, and I5 enable G5. When FFl set;, G5 is activated which genetates AWST-N . To select the data register, A01A-P and A02A-P are low and A03A-P is high. G6 is enabled by the outputs of I2 and I3 and A03A-P. When FF1 is set, G6 will be activated which generates ADAT-P. Gate G3 will be disabled if the correct combination of A01A-P, A02A-P and A03A-P are received to select one of the Parallel I/O internal registers.

5-389. To perform a write operation to the Parallel I/O data register, the master function generates the address (waveform A, figure 42), data, and strobe on the INFIBUS and generates RITE-N (waveform B, figure 42). The address will be recognized which enables FFl to be set, as explained previously. G3 generates AABL-P (waveform C, figure 42) and enables the set input of flip-flop FF2. RITE-N is inverted by inverter I11 which enables G7 and G10. The output of I11 is also inverted by inverter I12 which disables gate G11 causing ARED-P to go low. If the Alarm Control and VF Comm Link is ready to accept data, WBAR-N is low which disables gate G7. The high output of G7 enables gate G8. The parallel I/O INFIBUS access circuit generates STRA-P (waveform D, figure 42) which is applied to driver DR2. The output of DR2 is coupled through driver DR3 then delayed 50 nsee by delay DL4. The output of DL4 activates gate G8 which triggers and sets FF1. If the Alarm Control and VF Comm Link function is not ready to accept data, WBAR-N from the read-write control status circuit is high which activates G7. The output of G7 now disables G8 until the Alarm Control and VF Comm Link Function is ready When ready, WBAR-N returns to low disabling G7 which activates G8.

5-390. The output of FF1, AMAS-P (waveform E, figure 42), activates G6 which generates ADAT-P (waveform F, figure 42). Inverter I6 inverts AMAS-P and the output of I6 is delayed 50 nsec by delay DL1. After the delay, inverter I7 triggers and sets FF2 which enables gate G9. The output of I7 also activates gate G10 which generates AWRT-P (waveform G, figure 42). AWRT-P loads the data register in the Parallel I/O data output and control register circuit. The output of I7 is also inverted by inverter I8 and the output of I8 is delayed 50 nsec by delay DL2. After the delay, G10 is disabled and the output of I8 is inverted by

inverter I9 which activates gate G9. G9 generates ADUN-N (waveform H, figure 42) which causes the Parallel I/O INFIBUS access circuit to generate DONE-N, indicating a completed data transfer. Inverter I10 then inverts the output of I9 and after the SO nsec delay of delay DL3, G9 is disabled which removes ADUN-N (high).

5-391. To perform a read operation of the data register, the master function places the Parallel I/O address on the address lines and RITE-N will be high. The address is recognized, G6 is enabled and G3 generates AABL-P as explained previously. I11 inverts the high RITE-N input and disables G7 and G10. Inverter I12 inverts the output of Ill and generates ARED-P (waveform A, figure 43) which enables gate G11.

5-392. The remainder of the read operation is similar to the write operation, except when I7 inverts the delayed output of I6, G11 is activated. G11 generates DRBB-N (waveform B, figure 43) and after I9 inverts the delayed output of I8, G9 is activated. I10 inverts the output of I9 which disables G11. 50 nsec later, G9 is disabled removing ADUN-N.

5-393. The control register write operation is similar to the data register write operation, except G4 is enabled as explained previously and then activated by AMAS-P which generates ACNT-N. ACNT-N activates gate GI3 which generates MPXB-P. The control register read operation is similar to the data register read operation, except ACNT-N is generated and G13 is activated which generates MPXB-P. MPXB-P is used by the Parallel I/O data input and selector circuit during the read operation to select the control register data to be placed on the INFIBUS data lines.

5-394. The status register write operation is similar to the other write operations, except G5 is activated. G5 generates AWST-N to the Parallel I/O data output and control register circuit which generates the general reset for the Parallel I/O function. AWST-N activates gate G12 which generates MPXA-P. The status register read operation is similar to the other read operations, except when AWST-N is generated by G5, G12 is activated. The output of G12, MPXA-P, is routed to the Parallel I/O data output and selector circuit to select the status data that is to be placed on the INFIBUS data lines.

5-395. When the Parallel I/O INFIBUS access circuit is requesting INFIBUS access, BONE-N is low. BONE-N activates G12 and G13 which generate MPXA-P and MPXB-P, respectively. With MPXA-P and MPXB-P both high, the Parallel I/O data output and control register circuit generates the Parallel I/O device number which is strobed to the INFIBUS data lines.

5-396. PARALLEL I/O AlA3A10 INFIBUS ACCESS CIRCUIT.

5-397. General. The Parallel I/O INFIBUS access circuit generates a level 1 interrupt INFIBUS access request and, under control of the Bus Controller, allows the Parallel I/O to gain INFIBUS access. The level 1 interrupt is generated whenever the Parallel I/0 requests the INFIBUS to transfer data or whenever the Parallel I/O detects an error during a data transfer.

5-398. Detail Analysis (see figure 44). Initially, the Parallel I/O data output and control register circuit generates GRSA-N which clears the Parallel I/O INFIBUS access logic circuit. GRSA-N is generated when a master reset pulse, MRES-N, is received or when a write status register operation occurs. GRSA-N clears flip-flops FF2 through FF5 and activates gate G11 which resets FFl.

5-399. When an INFIBUS access is required, the Parallel I/O data output and control register circuit generates CR2S-P (waveform A, figure 45) which enables FFl to be set when triggered. Whenever a word is to be written into or read from the Parallel I/O (under control of the stored software program), the Parallel I/O read/write control status circuit generates PDSA-N (waveform C, figure 45). Whenever the read/write control status circuit detects an error, EROR-N (waveform D, figure 45) is generated. PDSA-N or EROR-N activates gate Gl. The

output of Gl is inverted by inverter I1 which triggers FF1. The output of FFl activates gate G5 if SELl-N is high (no other function requesting INFIBUS access). The output of G5 sets FF2 and disables gates G2 and G6. The output of FF2 enables G2 and G6 and also activates gate G4. The output of G4 is coupled through driver DRl which generates SRLl-N (waveform E, figure 45).

5-400. The Bus Controller receives SRLl-N and returns SELl-N, (waveform F, figure 45) and the precedance pulse PCDA-P (waveform G, figure 45). SELl-N disables G5 which enables G6 and activates G2. Gate G3 is disabled by the output of G2. G3 is normally enabled and will couple PCDA-P to the INFIBUS as PCDB-P if an INFIBUS access is not being requested. When an INFIBUS access is being requested G3 is disabled and PCDB-P is not coupled to the INFIBUS.

5-401. PCDA-P, when received, activates G6 which disables gate G8 and sets FF3. The 0 output of FF3 disables gates G4 and G5 and is coupled through driver DR2 which generates SACK-N (waveform H, figure 45). The Bus Controller detects SACK-N and removes SELl-N. G5 is again enabled by SELl-N (high) but disabled by the 0 output of FF3. The 1 output of FF3 enables gate G8. When PCDA-P returns to low G6 is disabled and activates G8. The output of G8 clears FF2 which disables G2, G4, and G6. With G2 disabled, G3 is enabled and PCDA-P can be coupled to the INFIBUS. The 1 output of FF3 also activates gate G7. The output of G7 sets FF4 and activates gate G12. The 0 output of FF4 disables G5 and the 1 output of FF4 enables gates G9 and G13 and activates gate G14 (FFS cleared). G14 generates BONE-N (waveform I, figure 45) and activates G12 which generates BOLA-P (waveform J, figure 4.5). BOLA-P and BONE-N enable the device number to be strobed to the INFIBUS data lines. BOLA-P also enables gates G15 and G16 and is inverted by inverter I7. The output of I7 is delayed 50 nsec by delay DLl. The output of DLl activates G16 generating STRB-N (waveform K, figure 45).

5-402. STRB-N is inverted by inverter I8 which generates STRA-P (waveform L, figure 45). STRA-P activates gate G9 which clea FF3. The 0 output of FF3 enables G4 and G5 and the i output of FF3 disables G7 and G8. Clearing FF3 causes SACK-N to return to high. After data is transferred, DONE-N (waveform M, figure 45) is received. DONE-N is inverted by inveter I3 which generates BDNA-P (waveform N, figure 45) BDNA-P activates G13, G14, and is also inverted by inverter I2. The output of Gl3 sets FF5 and activates G11 which resets FFl. The output of I2 disables gates G7 and G10. With FF5 set, G10 is enabled and when DONE-N is removed, BDNA-P will go low which disables G13 arid G14. The output of I2 now activates G10 which clears FF4. The output of G14 (high) disables G12 which causes BOLA-P to go low. BOLA-P now disables G16 which removes STRB-N. Clearing FF4 disables G9 and G14, clears FF5, and enables G5.

5-403. If DONE-N is not received within 2 usec after STRB-N goes low, the Bus Controller generates QUIT-N. Inverter I4 inverts QUIT-N which activates gate G15 (G15 enabled by BOLA-P during the normal cycle). The output of G15 clears FF3 and FF4 and activates G11 which resets FFl. Inverter 15 inverts the output of I4 which disables G7 to allow G15 to clear FF4.

5-404. PARALLEL I/O A1A3A10 DATA INPUT AND SELECTOR CIRCUIT.

5-405. General. The Parallel I/O data input and selector circuit receives data from the Alarm Control and VF Comm Link function and selects the data that is to be placed on the INFIBUS data lines. Data from the Alarm Control and VF Comm Link is temporarily stored by the data input register and the data selectors select one of four following data input groups: data from the Alarm Control and VF Comm Link function, control register contents, anti Parallel l/O status, or the Parallel I/O address (device number).

5-406. Detail Analysis (see figure 46). The input data register is controlled by the

Alarm Control and VF Comm Link. It comprises 20 flip-flops with flip-flop FFl shown. The 20 flip-flops are simultaneously clocked by RDST-N. The input data register receives ID00-P though ID11-P from the Alarm Control and VF Comm Link. The input data strobe IDSB-N (waveform A, figure 47) triggers single-shot SS1. The 1 output of SS1 (waveform B, figure 47) triggers SS2 which generates RDSP-P (waveform C, figure 47) and RDST-N (waveform D, figure 47). RDSP-P and RDST-N are routed to the Parallel I/O read/write control status circuit. RDST-N also clocks and loads the input data flip-flops with the input data (ID00-P through ID11-P) which generates RR00-N through RR15-N, as required. RR12-N through RR15-N and STS5-N through STS8-N are always genera ted.

5-407. All data to be placed on the INFIBUS data lines is 'first selected by the data selectors M1 through M6. Ml through M4 are dual four-line to one-line selectors whose output data is determined by the value of MPXA-P and MPXB-P. MS and M6 are each quad two-line to one-line selectors. The output data of M6 is determined by the value of MPXA-P. The output data of MS is determined by the value of BOLA-P.

5-408. When the Parallel I/O is slaved to read the data from the Alarm Control and VF Comm Link function, MPXA-P, MPXB-P and BOLA-P are low. Ml through M4 couple the lC0 and 2C0 inputs to the Yl and Y2 outputs, respectively. M5 and M6 couple the 1A through 4A inputs to the Yl through Y4 outputs, respectively. This condition couples the data from input data register, RROO-N through RR15-N, to the data output and control register circuit (DOOA-N through D15A-N).

5-409. When the Parallel I/O is slaved to read the Parallel I/O control register data from the Parallel I/O data output and control register circuit, the Parallel I/Q address receivers and recognition circuit generates MPXB-P (MPXA-P and BOLA-P low). M1 through M4 couple the lC2 and 2C2 inputs to the Yl and Y2 outputs, respectively. M5 and M6 couple the 1A through 4A inputs to the Yl through Y4, output, respectively. This condition couples the control register data to the Parallel I/O data output and control register circuit.

5-410. When the Parallel I/O is slaved to read status data, the Parallel I/O address receivers and recognition circuit generates MPXA-P (MPXB-P and BOLA-P low). Ml through M4 couples the 1C1 and 2Cl inputs to the Yl and Y2 outputs, respectively. MS couples the 1A through 4A inputs to the Yl through Y4 outputs, respectively. M6 couples the 1B through 4B inputs to the Yl through Y4 outputs, respectively. This condition couples the Parallel I/O and Alarm Control and VF Comm Link function status data to the Parallel I/O data output and control register circuit..

5-411. When the device number is to be placed on the INFIBUS data lines during an interrupt request, the Parallel I/O address receivers anti recognition circuit generates MPXA-P and MPXB-P, and the Parallel I/O INFIBUS access circuit generates BOLA-P. Ml through M4 couple the lC3 and 2C3 inputs to the Yl and Y2 outputs, respectively. MS couples the 1B through 4B inputs to the Yl through Y4 outputs, respectively. This condition couples the device number, DN04-N through DN11-N and STS5 through STS8, to the Parallel I/O data output and control register circuit.

5-412. PARALLEL I/O DATA OUTPUT AND CONTROL REGISTER CIRCUIT.

5-413. General. The Parallel I/O data output and control register circuit stores data that is to be transferred to the Alarm Control and VF Comm Link Function. Also, the Parallel I/O data output and control register circuit stores control words which controls read or write operations that are to be done with the Alarm Control and VF Comm Link Function.

5-414. Detail Analysis (see figure 48). When master reset, MRES-N, is generated on the INFIBUS I10 inverts MRES-N and the output of I10 activates gate G8 which generates GRSA-N. GRSA-N is in-

verted by inverter Ill which generates GRSC-P. Or, when the Parallel I/O is slaved to write its status register, the Parallel I/O address receiver and recognition circuit generates AWST-N (waveform A, figure 49) and AWRT-P (waveform B, figure 49). AWST-N enables gate G10 and AWRT-P is inverted by inverter I13 which activates G10. The output of G10 activates G8 which generates GRSA-N (waveform C, figure 49) and I11 generates GRSC-P (waveform D, figure 49). GRSA-N and GRSC-P are routed to the Parallel I/O read/write control status circuit for reset purpose. This causes the Parallel I/O read/write control status circuit to generate WBAS-P (waveform E, figure 49) which enables gate G9. GRSA-N also resets control register U66 (flip-f lop FF2 shown).

5-415. When the Parallel I/O is slaved to read out its status register, the Parallel I/O address receiver and recognition circuit generates AABL-P (waveform A, figure 50) and ARED-P (waveform B, figure 50) which enables gate G14. The Parallel I/O INFIBUS access circuit generates STRA-P (waveform C, figure 50) which activates G14. The output of G14 enables gates G12, G13 and G15. The parallel I/O address receiver and recognition circuit then generates AMAS-P (waveform D, figure 50) and AWST-N (waveform E, figure 50). AMAS-P activates G12 which generates DBRA-P (waveform F, figure 50). AWST-N is inverted by inverter I14 which activates G15 and G15 generates DBRC-P (waveform G, figure 50). At the same time, the Parallel I/O data input and selector circuit generates DOOA-N through Dl5A-N (representing status data) which are routed to the data bus drivers/receivers U69, U70, U79, and U80. DBRA-P strobes data bus driver/receiver U70 and U80 which couples DOOA-P through DOSA-N, D08A-N, and DOSA-N to the INFIBUS data lines DBOO-N through DBOS-N, DBOI-N, and DBO9-N. DBRC-P strobes data bus driver U79 which couples Dl2A-N through D15A-N to the INFIBUS data lines DB12-N through DB15-N. After the transfer is completed, STRA-P is removed which causes the status data to be removed from the INFIBUS.

5-416. When the Parallel I/O is slaved to load a write operation control word into the control register, DBOO-N through DB05 -N, representing the control word are on the INFIBUS. DBOO-N through DBOS-N are inverted by data bus driver/receiver U80 and routed to the inputs of control register U66. Inverter I7 and gates G4 and G7 decode the inverted DBOO-N and DBOl-N bits. For a write operation, both DBOO-N and DBOl-N are low which causes G4 to be disabled and G7 to be activated. G4 presents a low and G7 presents a high to the inputs of control register U66. The Parallel I/O address receiver and recognition circuit generates ACNT-N (waveform A, figure 51) which enables gate G11. Afterwards, the Parallel I/O address receiver and recognition circuit generates AWRT-P (waveform B, figure 51) which is inverted by I13. The output of I13 activates G11 which generates WRCO-P (waveform C, figure 51). WRCO-P triggers and loads the control register U66 with the control word. Also, WCRO-P is routed to the Parallel I/O, read/write control status circuit.

5-417. The control register U66 generates CRlS-P (waveform D, figure 51) for a write operation and CR2S-P (waveform E, figure 51) which is routed to the Parallel I/O INFIBUS access circuit to enable interrupts. Also, gate G2 and inverters I3 through I6 and I8 invert the outputs of control register U66 and generate CROO-N through CRO5-N (waveform F, figure 51) which are routed to the Parallel I/O data input and selector circuit.

5-418. When the Parallel I/O is slaved to load a read operation control word into the control register, the cycle performed is similar to the cycle performed when loading a write operation control word. The difference is that for a read operation control word DBOO-N is low and DBOl-N is high (on the INFIBUS) which causes G4 to be activated and G7 to be disabled. G4

generates CROA-P (waveform A, figure 52) which is routed to the input of control register U66 (FF2 shown) and to the Parallel I/O read/write control status circuit. When ACNT-N (waveform C, figure 52) and AWRT-P (waveform D, figure 52) are generated, G11 is activated which generates WRCQ-P (waveform D, figure 52), As discussed, WRCO-P triggers and loads control register U66 with the read control word and the control register generates CROS-P (waveform E, figure 52) which is routed to the Parallel I/O read/write control status circuit. CR2S-P is generated to enable interrupts as discussed.

5-419. When the Parallel I/O is slaved to read its control register, the Parallel I/O address receives and recognition circuit generates AABL-P and ARED-P which enable G14. The Parallel I/O INFIBUS access circuit then generates STRA-P which activates G14. The output of Gl4 enables G12, G13 and G15. The Parallel I/O address receiver and recognition circuit then generates AMAS-P which activates G12 causing DBRA-P to be generated. At the same time, the Parallel I/O data input and selector circuit generates DOOA-N through D15A-N, representing the control word, which is routed to data bus driver/receivers U69, U70, U79 and U80. DBRA-P strobes data bus driver/receivers U70 and U80 which couple DOOA-N through DO5A-N, DO8A-N, and D09A-P to the INFIBUS data lines, DBOO-N through DB05-N, DB08-N, and DB09-N.

5-420. To have data loaded into the Parallel I/O data register, the Parallel I/O must first be reset. Then the Parallel I/O control register is loaded with a write control word. This causes WBAS-P (waveform A, figure 53) and CRlS-P (waveform B, figure 53) to be generated, as discussed previously, which enables G9. When the Parallel I/O is slaved to write data into its data register, DBOO-N through DB11-P, representing the data word, are present on the INFIBUS. DB00-N through DB11-N are inverted and routed to the output data register U57 and U76 by data bus driver/receivers U69, U70 and U80. The Parallel I/O address receiver and recognition circuit then generates ADAT-P (waveform C, figure 53) and AWRT-P (waveform D, figure 53). ADAT-P enables G9 and AWRT-P activates G9 which generates WDBR-N (waveform E, figure 53). WDBR-N triggers and loads the output data register U57 and U76 with the data word. Also, WDBR-N is routed to the Parallel I/O read/write control circuit. This causes WBAS-P (waveform A, figure 53) to be removed which disables G9. G9 removes WDBR-N (waveform E, figure 53) and the outputs of the output data registers U57 and U76 are coupled through data drivers U62, U63 and U72 (DRI shown) which generates ODOO-P through OD11-P (waveform F, figure 53). ODOO-P through OD11-P represents the data word which is routed to the Alarm Control and VF Comm Link Function.

5-421. When the Parallel I/O is slaved to read data out of its data register, the Parallel I/O address receiver and recognition circuit generates AABL-P (waveform A, figure 54) and ARED-P (waveform B, figure 54). AABL-P and ARED-P enable G14. The Parallel I/O INFIBUS access circuit then generates STRA-P (waveform C, figure 54) which activates G14. The output of Gl4 enables G12, G13 and G15. The Parallel I/O address receivers then generate AMAS-P (waveform D, figure 54) and ADAT-P (waveform E, figure 54). AMAS-P activates G12 which generates DBRA-P (waveform F, figure 54) and ADAT-P activates G13 and G15 which generates DBRB-P (waveform G, figure 54) and DBRC-P (waveform H, figure 54), respectively. At the same time, the Parallel I/O data input and selector circuit generates DOOA-N through D15A-N , representing data, which are routed to data bus driver/receivers U69, U70, U79, and U80. DBRA-P, DBRB-P, and DBRC-P strobes the data bus driver/receivers which cause the data to be routed onto the INFIBUS data lines DBOO-N through DBl5-N.

5-422. When the Parallel I/O performs an interrupt, the Parallel I/O address (device number) is placed on to the INFIBUS data lines. The Parallel I/O INFIBUS access circuit generates BOLA-P and BOLA-P activates G12, G13 and G15

which generates DBRA-P, DBRB-P, and DBRC-P, respectively. At the same time, the Parallel I/O data input and selector circuit generates DOOA-N through Dl5A-N, representing the Parallel I/O address, which are routed to data bus driver/receivers U69, U70, U79 and U80, DBRA-P, DBRB-P, and DBRC-P strobe data bus driver/receivers U69, U70, U79, and U80 which couples DOOA-N through D15A-N to INFIBUS data lines DBOO-N through DB15-N.

5-423. PARALLEL I/O READ/WRITE CONTROL STATUS CIRCUIT.

5-424. General. The Parallel I/O read/write control status circuit controls the transferring of data to or from the Alarm Control and VF Comm Link. It controls read and write operations with the Alarm Control and VF Comm Link and provides error indications for timing errors and overrun conditions.

5-425. Detail Analysis (see figure 55). When the master reset pulse is generated on the INFIBUS or when the Parallel I/O status register is written, the Parallel I/O data output and control register circuit generates GRSA-K (waveform A, figure 56) and GRSC-P (waveform B, figure 56). GRSA-N resets flip-flop FF4 and activates gate G8 which resets flip-flop FF3. GRSC-P activates gate G2 and the output of G2 presets flip-flop FFl. FFl then generates WBAR-N (waveform C, figure 56) and WBAS-P (waveform D, figure 56). WBAR-N disables gates G4 and G6, and WBAS-P enables gate G13.

5-426. When a write control word is loaded in the Parallel I/O data output and control register circuit, CR1S-P (waveform E, figure 56) is generated. CRlS-P enables gates G4 and G14 and activates gate G13. The output of G13 generates PDSA-N.

5-427. PDSA-N is routed to the Parallel I/O INFIBUS access circuit which causes it to initiate an interrupt. WDDC-N from the Alarm Control and VF Comm Link is normally a high, which activated exclusive-OR gate G1. The output of Gl enables G4. When the Parallel I/O is presented with a data word, the Parallel I/O data output and control register circuit generated WDRB-N. WDRB-N triggers and clears FFl which removes WBAR-N/WBAS-P. With WBAS-P low. G13 is disabled causing PDSA-N to be removed, With WBAR-N high, G4 and G6 is activated. G6 triggers single-shot SS2 which remains set for 2.0 usec. The output of G4 activated ate G5, The output of G5 is inverterted by inverter I1 which generates WDGA-N. WDGA-N is routed to the Alarm Control and VF Comm Link.

5-428. When the Alarm Control and VF Comm Link is ready to accept the data word, WDDC-P is generated which activates exclusive-OR gate Gl. The output of G1 activates G4 and the output of G4 activates gate G5. The output of G5 is inverted by inverter I1 which generates WDGA-N (waveform I, figure 56). WDGA-N is routed to the Alarm Control and VF Comm Link.

5-429. After 2.0 usec, SS2 resets and triggers single-shot SS3. The 0 output of SS3 is inverted by inverter I2 which generates WDST-P (waveform J, figure 56). WDST-P is routed to the Alarm Control and VF Comm Link causing it to accept the data word. The Alarm Control and YF Comm Link removes WDDC-P which disables G1. The high-to-Low transition output of G1 triggers SSl. The 1 output of SSl activates G2 which presets FF1. FFl generates WBAS-P and WBAR-N and the cycle for- transferring data to the Alarm Control and VF Comm Link is repeated for the next data word.

5-430. When the Parallel I/O control register is loaded with a read operation control word, the Parallel I/0 data output and control register circuit generates WRCO=P (waveform A, figure 57), CROA-P (waveform B, figure 57), and CROS-P (waveform C, figure 57). WRCO-P and CROA-P activate gate G3 which presets flip-flop FF2. CROS-P enables G13 and the set input of FF2.

5-431. The 1 output of FF2 is inverted by inverter I3, triggers single-shot SS4, and enables G9 after a 50 nsec delay by DLl. I3 generates RDRC-N (waveform D, figure 57) and SS4 disables gate G9 for 300 msec. The 1 output of FF2 is inverted by inverter J4 which generates RDRC-N (waveform E, figure 57). RDRC-N is routed to the Alarm Control and VF Comm Link to initiate a read operation.

5-432. If the Alarm Control and VF Comm Link ES not ready to accept the data word, it generates WDNR-N, STSl-N, and STS2-N. WDNR-N activates gate Gl5, and STSl-N and STS2-N disable G6. The output of G15 activates G14 which generates EROR-N. EROR-N is routed to the Parallel I/O INFIBUS access circuit to initiate an interrupt for the error. The output of G15 is inverted by inverter I5 which generates WDNR-N. WDNR-N disables G4 and G6 and is also routed to the Parallel I/O data input and selector circuit.

5-433. The Alarm Control and VF Comm Link presents a data word to the parallel I/O which causes the data input and selector circuit to generate RDST-N (waveform F, figure 57) and RDSP-P (waveform G, figure 57). RDSP-P triggers FF4 (FF4 remains cleared), and activates gate G10 which resets FF2. This causes RDRC-N and RDRH-P to be removed and G9 to be disabled 50 nsec after FF2 is reset.

5-434. RDST-N and RDSP-P are removed after 1.0 usec causing RF3 to be triggered and set, and G10 to be disabled. The 1 output of FF3 enables the set input of FF4 and also, activate G13. The output of G13 is coupled through DR1 which generates PDSA-N. PDSA-N is routed to the Parallel I/O INFIBUS access circuit. The Parallel I/O INFIBUS access circuit initiates an interrupt to have the data word read out. When the Parallel I/O is slaved to have the data word read out, the Parallel I/O address receiver and recognition circuit generates DRBB-N (waveform I, figure 57). DRBB-N activates G8 which resets FF3, causing PDSA-N to be removed. When DRBB-N is removed, G8 is disabled which triggers and sets FF2. This causes RDRC-N and RDRH-P to be generated. This cycle is repeated for each data word to be transferred.

5-435. If the Alarm Control and VF Comm Link is not ready to have a data word read out, it generates RDNA-N. RDNA-N disables gate G11 which generates RDNR-N. RDNR-N disables the set input of FF3 and activates G12 which activates G10 and G14. The output of G10 resets FF2 and G14 generates EROR-N. EROR-N is routed to the Parallel I/O INFIBUS access circuit to initiate an interrupt to indicate the Alarm Control and VP Comm Link is not ready.

5-436. If the Alarm Control and VF Comm Link does not present the data word within 300 msec after SS4 is triggered, SS4 resets which activates G9. The output of G9 presets FF4 which generates RTER-N which is routed to the Parallel I/O data input and selector circuit. RTER-N also activates gate G12 which activates G10 and G14. G10 resets FF2 and G14 generates EROR-N which is routed to the Parallel I/O INFIBUS access circuit. The Parallel I/O INFIBUS access circuit initiates an interrupt to indicate a read timing error.

5-437. If the previous data word presented by the Alarm Control and VF Comm Link is not read out of the Parallel I/O before the next data word is presented, the previous word is destroyed and a read timing error occurs. FF3 is not reset by G8, as explained previously, which holds the set input of FF4 enabled. When RDSP-P is generated by the Parallel I/O data input and selector circuit, FF4 is triggered and set which generates RTER-N. As explained previously, EROR-N is generated which initiates an interrupt to indicate an overrun error.

5-438. SERIAL I/O CONTROL GROUP ADDRESS RECOGNITION CIRCUIT.

5-439. General. The address recognition circuit recognizes the Serial I/O address (device number) that is placed on the INFIBUS address lines when slaved by a master function. It decodes a portion of the address to select any of the three internal registers and depending on the condition of the RITE-N line, it performs a read or write cycle.

5-440. The TTY Controller is assigned address F8OX l6 where X is any hexidecimal number between 0 and F which allows the appropriate internal register to be addressed.

Whenaddress F8OX l6 (1,1,1,1,/1,0,0,0,/ 0,0,0,0,/X,X,X,X,) is sensed on the INFI-BUS address lines, address recognition occurs and the operation determined by the condition of the RITE-N line and the internal register selected is performed.

5-441. The Modem Controller 1 is assigned address F93X l6 where X is any hexidecimal number between 0 and F which allows the appropriate internal register to be addressed. Whenaddress F93X l6 (1,1,1,1,/1,0,0,1,/ 0,0,1,1,/X,X,X,X,) is sensed on the INFI-BUS address lines, address recognition occurs and the operation determined by the condition of the RITE-N line and the internal register selected is performed.

5-442. The Printer Controller (ACOC Group only) is assigned address F8lX l6 where X is any hexidecimal number between 0 and F which allows the appropriate internal register to be addressed. When address F81X 16 (l,l,l,l,/1,0,0,0,/0,0,0,1,/ X,X,X,X,) is sensed on the INFIBUS address lines, address recognition occurs and the operation determined by the condition of the RITE-N line and the internal register selected is performed.

5-443. The Modem Controller 2 (ACOC Group only) is assigned address F94X l6 where X is any hexidecimal number between 0 and F which allows the appropriate internal register to be addressed. When address F94X 16 (1,1,1,1,/1,0,0,1,/0,1,0,0,/ X,X,X,X,) is sensed on the INFIBUS address lines, address recognition occurs and the operation determined by the condition of the RITE-N line and the internal register selected is performed.

5-444. Each of the four Serial I/O's have three internal registers; the status register, control register, and data register. When X is equal to 0 (O,O,O,O,) the status register of the selected Serial I/O is addressed. When X is equal to 6 (0, 1, 1, 0,) the control register of the selected Serial I/O is addressed. When X is equal to 8 (l,O,O,O,) the data register of the selected Serial I/O is addressed.

5-445. Detail Analysis (see figure 58). The address bus receivers (11 shown) invert ABOl-N through ABI5-N (ABOO-N, 0 bit position is not used for function address). Inverted AB04-N through AB11-N are applied to the address comparators (Gl shown) where it will be compared with the jumper encoded address, DN04-P through DN11-P (device number), from the data selector/ control circuit, AB12 -N through ABl5-N are low for Serial I/O control group function addresses. Inverted ABOl-N through AB03-N are decoded to select one of the three internal registers.

5-446. A typical operation starts with the status register being written into which clears the selected Serial I/O. Afterwards, under control of the stored software program, status is tested (read out) by the master function to check the condition of the selected Serial I/O and the external device. The control register is then loaded with the read or write operation to be performed with the external device being slaved.

5-447. If a write operation is to be performed, the Serial I/O is slaved (addressed) to select the data register which is then loaded with the data. With the write operation loaded into the control register, the selected Serial I/O function presents the data to the external device. If a read operation is to be performed, the selected Serial I/O function will strobe the data to the INFIBUS data lines.

5-448. The data selector/control circuit always applies the jumper encoded device number, DN04-P through DN11-P, to the address comparators. The inverted AB04-N through ABl l-N inputs are compared with the jumper encoded device number and if a match occurs, the set input of flip-flop FF1 will be enabled. When both inputs to each of the address comparators are at the same level, the output will be high. All of the outputs of the address comparators, gate G3 and driver DRl must be high for the set input of FF1 to be enabled.

5-449. Initially, a master function slaves the selected Serial I/O to clear the selected

serial I/O by writing into the status register. The address, AB0l-N through ABl5-N (figure 59, waveform A), and RITE-N (waveform B, figure 59) are placed on the INFIBUS. The selected Serial I/O status register address, FXYO 16 is generated where X and Y make up the variable device number (AB04-N through AB11-N). The inverted AB04-N through AB11-N inputs are applied to the address comparators and inverted AB12-N through AB14-N input activate G3. The inverted ABl5-N input is coupled through DRl and with the output of G3 and the address comparators high, the set input of FFl high. At the same time, with ABOl-N through AB03-N high and inverted by inverters 12, 14 and 16 which enables gate G5. If ABOl-N through AB03-N are not a valid register address, gate G2 is activated. The output of G2, AILA-P, is low which disables the set input of FF2. When a valid address is detected, G2 is disabled and AILA-P is high. At the same time, Inverter I7 inverts RITE-N, generating RITA-P (waveform C, figure 59). RITA-P enables gates G10, G13, G15 and G18. Inverter I16 inverts RITA-P which disables gates G16 and Gl9. STRC-P (waveform E, figure 59) from the Serial I/O Control Group INFIBUS access circuit is coupled through driver DR2 which activates gate G9. The output G9 triggers and sets FFl. AMAS-P (waveform F, figure 59) is generated by FFl which activates G5. Inverter I3 inverts the output of G5 generating ASUS-P (waveform G, figure 59). The output G5 also activates gate G8 which **generates** MPXA-P. AMAS-P is inverted by inverter I8, disables the reset input of flip-flop FF2 and enables gate G20. At this time, AILA-P is high (valid address) and the set input of FF2 is enabled. After the 50 nsec delay of delay DLl, Inverter I9 inverts the delayed output of I8 and triggers and sets FF2. The output of I9 also activates gate G11. The output of G11 activates Gl5 which activates gate G14. The **output** of G14 is inverted by inverter I15 which generates ARES-N (waveform H, figure 59). ARES-N resets the infibus access circuit, control register circuit, asynchronous data transfer control circuit and data selector/control circuit. The high **output** of I9 is also inverted by inverter I10. The **low output** of I10 is delayed 50 nsec by delay DL2. The delayed output of DL2 disables G11 which disables G15 causing ARES-N to return to high. At this time, the 1 output of FF2 enables gate G12 and inverter Ill inverts the low output of DL2 which activates G12. The output of G12, ADUN-N (waveform I, figure 59), is generated for 50 nsec. The high output of Ill is inverted by inverter I12I then delayed 50 nsec by delay DL3 which disables G12. ADUN-N is routed to the INFIBUS access circuit where it will generate DONE-N to indicate a completion to the master function.

5-450. To read the status register of the Serial I/O, the cycle is similar to a status **register write** except RITE-N (waveform B, figure 60) and its inverse RITA-P (waveform C, figure 60) are not generated. AILA-P (waveform D, figure 60) must be present to indicate a valid address and STRA-P (waveform F, figure 60) is generated at the same time as STRC-P (waveform E, figure 60). STRA-P enables G20. ASUS-P and MPXA-P are generated as explained previously. MPXA-P selects the status data in the data selector/control circuit. With RITA-P low, G13, G15, and G18 are disabled. RITA-P is also inverted by I16 which enables G16 and activates Gl9. The output of G19 enables G20 and when AMAS-P is generated, as explained previously, G20 is activated generating BDIN-P (waveform J, figure 60). BDIN-N is routed to the data selector/control circuit to strobe the status data to the infibus data lines. G11 will be activated 50 nsec after AMAS-P is generated but does not activate any gates. ADUN-N (waveform K, figure 60) is generated as explained previously.

5-451. After the status register is read, the control register is loaded (written into) for a read or write operation with the external device being controlled by the Serial I/O function. The address recognition cycle is the same as discussed except, gate G6 will be activated for a control register address. RITE-N, RITA-P, AILA-P, STRC-P, STRA-P, and AMAS-P (waveforms A through G, figure 61) are generated as explained previously. The output of G6 is inverted by lnverter I5 which generates ACNT-P

(waveform H, figure 61). The output of G6 also activates gate G7 which generates MPXB-P. (MPXB-P is not used for a control register write cycle.) ACNT-P and RITA-P enables G13. When G11 is activated, as explained previously, G13 is activated which generates ALDC-P (waveform I, figure 61). ALDC-P is routed out to the control register circuit to clock the control register. The control register will then be loaded with the data present on the INFIBUS lines. ADUN-N (waveform J, figure 61) is generated as explained previously.

5-452. To read data from the control register, the master function address the Serial I/O with the control register address but RITE-N (waveform B, figure 62) is not generated. With RITA-P (waveform C, figure 62) low G10, G13, Gl5 and G18 are disabled. I16 inverts the RITA-P (low) which enables G16 and activates G19. AILA-P (waveform D, figure 62) and STRC-P (waveform E, figure 62) are generated as explained previously. STRA-P (waveform F, figure 62) enables G20. When FFl is set, AMAS-P (waveform G, figure 62) activates G20 which generates BDIN-P (waveform J, figure 62). G6 is activated, as explained previously, which activates G7, generating MPXB-P (waveform I, figure 62), to the data selector/control circuit. I5 inverts the output of G6 which generates ACNT-P (waveform H, figure 62); however, ACNT-N is not used during a read cycle. MPXB-P selects the control register contents in the data selector/control circuit and BDIN-P strobes the control register data to the INFIBUS data line:; - ADUN-N (-waveform K, figure 62) is generated as explained previously.

5-453. To write data into the data register, the master function will address the Serial I/O function with FXY8 16. The X and Y represents the variable Serial I/O address and 8 represents the address of the data register. Address data, and RITE-N (waveform B, figure 63) is placed on the INFIBUS by the master function. RITE-N enables G16 and G18 and RITA-F (waveform C, figure 63) enables G13, Gl5, G16, and G18. I16 inverts RITA-P which disables G16 and G19. AILA-P, STRC-F, STRA-P, and AMAS-P (waveforms D through G, figure 63) are generated as explained previously. With the data register addressed gate G4 is activated which generates ADAT-P (waveform H, figure 63). ADAT-P enables G16 and activates G18. The output of G18 enables G17. When G11 is activated as explained previously, G17 is activated. The output of G17, AOCK-N (waveform I, figure 63), is routed to the asynchronous data transfer control circuit and data selector/control circuit to clock the data into the data register. ADUN-N (waveform J, figure 63) is generated as explained previously.

5-454. To read the contents of the data register RITE-N, RITA-P, AIZA-P, STRC-P, STRA-P, and AMAS-P (waveforms B through G, figure 64) are generated as explained previously. ADAT-P (waveform H, figure 64), is generated which enables G16 and G18. PITE-N is high for a read cycle and with RITA-P low G10, G13, G15 and G18 are disabled. I16 enables G16 and G19. With AILA-P high for a valid address, G19 is activated which enables G20. STRA-P and AMAS-P activates G20 which generates BDIN-P (waveform I, figure 64) to the data selector/control circuit. BDIN-P strobes the data register data to the INFIBUS data lines. When Gil is activated as explained previously, G16 is activated which generates RCBA-N (waveform J, figure 64). RCBA-N is routed out to the asynchronous data transfer control circuit for reset purposes. During a read cycle of the data register, MPXA-P and MPXB-P are not generated which selects the data register contents in the data selector/control circuit. ADUN-N (waveform K, figure 64) is genera ted a s explained previously.

5-455. During an INFIBUS access cycle, BONE-N activates G7 and G8 which generates MFXA-P and MPXB-P. MPXA-P and MFXB-P cause the device number to be generated to the INFIEUS during the INFIBUS access cycle.

5-456. The master reset pulse, MRES-N, is inverted by inverters I13 and I14. The output of I14 activates G14 and the output of G14 is inverted by I15 which generates ARES-N.

5-457. SERIAL I/O CONTROL GROUP INFIBUS ACCESS CIRCUIT.

5-458. General. The INFIBUS access circuit performs the function of obtaining access to the INFIBUS on the assigned interrupt level when data is to be transferred or when an error, while transferring data, has occurred.

5-459. Detail Analysis (see figure 65). When the master reset pulse is generated on the INFIBUS or when the status register is written, the address recognition circuit generates ARES-N. ARES-N clears flip-flops FF2 through FF5 and activates gate G8 which resets flip-flop FFl.

5-460. When a control word, enabling interrupts, is stored in the control register of the control register circuit, BALS-P is generated by the control register circuit which enables the set input of FFl. BTRQ or EROR-N (waveform A, figure 66) from the asynchronous data transfer circuit activates gate Gl which triggers and sets FFl.

5-461. Deleted.

5-462. The Bus Controller senses SRL2-N and generates SEL2-N and PCDA-P. SEL2-N disables G2 and the output of G2 (high) enables G3 and activates G14 which disables gate G16. PCDA-P, when received, activates G3 which disables gate G5 and sets FF3. The 0 output of FF3 disables G2 and G15 and is coupled through driver DRl which generates SACK-N. The output of G15 is coupled through DR4 which removes SRL2-N.

5-463. SACK-N is sensed by the Bus Controller which causes the bus Controller to remove SEL2-N. When PCDA-P goes low, G3 is disabled and the output of G3 (high) activates G5 which clears FF2. The 1 output of FF2 disables G3, G14, and G15. G16, enabled by the high output of G14, couples PCDA-P to the INFIBUS or PCDB-P.

5-464. The 1 output of FF3 enables G5 and activates gate G4 which sets FF4 and activates gate G10. G10 generates BOLA-P (waveform F, figure 66) which is routed to the data selector/control circuit and address recognition circuit. The 0 output of FF4 disables G2 and the 1 output of FF4 enables gate G6 and G9 and activates G11. G11 generates BONE-N (waveform G, figure 66) which activate G10 and is routed to the address recognition circuit. BOLA-P also enables gates G12 and G13 and is inverted by inverter I5.
The output of I5 (low) is delayed 50 nsec by DLl and then activates G12 which generates STRB-N (waveform H, figure 66).

5-465. STRB-N is inverted by inverter I6 which generates STRA-P (waveform I, figure 66). STRA-P IS routed to the address recognition circuit and coupled through driver DR3 which generates STRC-P (waveform J, figure 66). STRC-P is routed to the address recognition circuit. STRA-P also activates G6 which clears FF3 and the 0 output of FF3 (high) is coupled through DRl which removes SACK-N. STRA-P is also inverted by inverter I1 which disables G4.

5-466. Normally, within 2 usec after STRB-N is generated, DONE-N (waveform K, figure 66) is generated by the master function receiving the interrupt. DONE-N is inverted by inverter I2 which activates G9 and G11. The output of I2 IS inverted by inverter I3 which disables G4 and G7. The output of G9 sets FF5 and activates G8 which resets FFl. The 1 output of FF5 enables G7. When DONE-S goes high, I2 disables G9 and G11, and the output of I3 activates G7 which clears FF4. The 1 output of FF4 (low) clears FF5 and with G11 disabled, G10 is disabled which disables (G12 and STRB-N is removed.

5-467. If the Bus Controller does not sense DONE-N within 2 usec, it generates QUIT-N which is inverted by I7. The output of I7

activates G13 which sets FF6. The output of I7 is also inverted by inverter I4 which disables G4. The 0 output of FF6 clears FF3 and FF4, and activates G8 which clears FFl.

5-468. When the address recognition circuit generates ADUN-N; ADUN-N is routed through driver DR2 which generates DONE-N on to the INFIBUS.

5-469. SERIAL I/O CONTROL GROUP CLOCK GENERATOR CIRCUIT.

5-470. General. The clock generator circuit is a psuedo random clock generator used to control the rate of data transfers (BAUD rate) to and from the external device. The TTY Controller and the Printer Controller (ACOC group only) do not use the clock generator logic. The TTY and Printer Controllers use an external variable clock that is coupled through the clock generator circuit. This external variable clock is used to vary the BAUD rate, synchronizing the TTY Controller or Printer Controller to the BAUD rate of the external device.

5-471. Detail Analysis (see figure 67). The TTY Controller and Printer Controller functions do not use the clock generator logic. The external variable clock, DSRI-P, from the TTY Controller or Printer Controller is coupled through inverters I2 and I3. The output of I3, CLCK-P, is routed to the data selector/control circuit, asynchronous data transfer circuit, and control register circuit.

5-472. The following discussion pertains to the Modem Controller 1 and 2 functions which receive CLKA-N from the INFIBUS. CLKA-N is a 25 MHz symmetrical signal and is applied to ‘divider U80 which divides CLKA-N by four (6.25 MHz).

5-473. Initially, dividers U72, U73, and U79 contain a random count. Inverter I1 inverts the output of divider U80 clocking dividers U72, U73, and U79. Divider U79 is always enabled and its carry output enables divider U73 to count. When dividers U79, U73 and U72 are fully loaded, Gl is activated which enables the load inputs of dividers U72, U73, and U79. On the next trigger, the three counters are preloaded. Divider U79 is loaded with binary coded 11 (1011) where the least significant bit positions is A and the most significant bit is D. Divider U73 is also loaded with 11 and divider U72 is loaded with 14.

5-474. After the dividers U72, U73 and U79 are preloaded, divider U79 will divide the output of I1 by five to step divider U73 once (11 to 12). At this time divider U79 is at zero and divider U73 is at a 12 count. Divider U79 is now a divide by 16 counter and divider U73 is effectively a divide by four counter. In order for divider U73 to step divider U72 once, divider U79 now divides the output of I1 by 16 and divider U73 divides by four. Divider U72 now steps to a count of 15 (1111) which causes the carry output to enable Gl and the QA output of divider U72 to go high. The QA output of divider U72 is inverted by I3 and the output of I3, CLCK-P, goes low. Therefore, in order to change the state of CLCK-P from the initial time (preloaded counters), the total division is four (U80) times five (U79) plus the result of four (USO) times I6 (U79) times four (U73), this equals a division of 276 and causes a CLCK-P pulse of 11.04 usec duration to be generated.

5-475. The clock pulse that caused divider U72 to step to a count of 15, also causes dividers U79 and U73 to return to a count of 0. With divider U73 at a count of 0, the carry output of divider U73 (low) prevents the carry output of divider U72 from being generated. Dividers U79 and U73 count 256 (1024 CLKA-N input pulses) additional input triggers. At this time, dividers U79, U73, and U72 are each at a count of 15 and the carry output of divider U79 enables Gl. The carry output of U79 also causes the carry output of divider U73 to be generated which causes the carry output of divider U72 to be generated. The carry output of divider U72 activates Gl. The next trigger input to the dividers U79, U73, and U72, with Gl activated, causes the divider to be preloaded, as explained previously, a second time. This sequence of events causes a 11.04 usec pulse to be generated at a 19.2 KHz rate (1200 band x 16).

5-476. SERIAL I/O CONTROL GROUP CONTROL REGISTER CIRCUIT.

5-477. General. The control register circuit stores control words (determined by stored software program) which commands the asynchronous data transfer control circuit to perform read or write operations.

5-478. Detail Analysis (see figure 68). When the master reset pulse is generated on the INFIBUS or when the status register is written, the address recognition circuit generates ARES-N. ARES-N clears control register U48 and resets control flip-flops FFl and FF2. RNIN-N and TNOT-N are generated by inverters I2 and I3, and routed to the asynchronous data transfer control circuit.

5-479. When the control register is written into, the data selector/control circuit presents the control word, DOOA-P through DOSA-P, and the address recognition circuit generates ALDC-P. ALDC-P clocks the control register and triggers the control flip-flops FFl and FF2. This causes the control word to be loaded into the control register U48, FFl and FF2.

5-480. DCOA-P and DOlA-P are decoded by inverter I1 and gates G3 and G4. When DOOA-P is high (read operation), G3 is activated. When DOOA-P and DOlA-P are high (write operation), G4 is activated.

5-481. Gates Gl, G2, G5, G6, single shot SS1, inverters I2 through I7, and transistor switch Q3 decodes the control word stored in the control register U48 and control flip-flops FFl and FF2. When a write control word is stored, TOTR-N, TOTS-P, TRSR-N, RRDR-N, TRAC-N, BARL-N, and TDRY-P can be generated and routed to the data selector/control circuit. Also RWIN-N, TOAK-P, TOTS-P and TOTR-N are generated and routed to the asynchronous data transfer control circuit.

5-482. When a read control word is stored, RINS-P, RLOP-P, TRAC-N, RLPR-N, and BARL-N can be generated and routed to the data selector/control circuit. Also, TNOT-N and RINS-P are generated and routed to the asynchronous data transfer control circuit.

5-483. SERIAL T/O CONTROL GROUP DATA SELECTOR/CONTROL CIRCUIT.

5-484. General. The data selector/control circuit stores data that is to be transmitted to the external device or received from the external device. Also, the data selector/control circuit selects the data that is to be placed on the INFIBUS.

5-485. Detail Analysis (see figure 69). When the master reset pulse is generated on the INFIBUS or when the Serial I/O status register is written, the address recognition circuit generates ARES-N. ARES-N activates gates G8 and G9 and presets flip-flop FF3. The outputs of G8 and G9 reset flip-flops FFl and FF2, respectively. FF3 generates DSTS-P and the 0 output of FF2 enables gate G3 and gate G5.

5-486. With a write operation control word stored in the control register circuit, TOTR-N, TOTS-P, TRSR-N, RRDR-N, TRAC-N, EARL-N and TDRY-P are generated. TOTS-P enables gate G5 and G10. TOTR-N, TOTS-P, TRSR-N, RRDR-N, TRAC-N, BARL-N and TDRY are routed to the input,: of data multiplexers U56, U58, and U67.

5-487. When the external device is ready to accept data, the asynchronous data transfer control circuit generates BTRQ-N which is routed to the 2Cl input of data multiplexer U56. Also, the INFIBUS access circuit initiates an interrupt and during the interrupt cycle, the INFIBUS access circuit generates BOLA-P and the address recognition circuit generates MPXA-P, MPXB-P, and BDIN-P.

5-488. The Serial I/O device number DN04-P through DNl l-P is routed to the address recognition circuit and also inverted by inverters I4 through I11. 14 through I7 generate DN04-N through DN07-N which is routed to the data multiplexers U67 and U78. The outputs of I8 through I11 are routed to the device number bus drivers U60.

5-489. MPXA-P and MPXB-P cause the data multiplexers U56, U58, U67 and U78

to couple the lC3 and 2C3 inputs and to the 1Y and 2Y outputs. This causes TOTR-N to generate DDOO-N, and DN04-N through DN07-N to generate DD04-N through DD07-N which are routed to the data bus driver/receivers U59 and U69.

5-490. BDIN-P strobes the data bus driver/receivers U59 and U60, and BOLA-P strobes the device number bus drivers U60 and U70. This causes the Serial I/O encoded device number to be strobed onto the INFIBUS data lines.

5-491. When the interrupt is serviced the Serial I/O is addressed to write data into the data register. Data from the INFIBUS, DBOO-N through DB07-N, is inverted by the data bus driver/receivers U59 and U69 inverters (11 shown) which generates DOOA-P through D07A-P. DOOO-P through D007-P are routed to the parallel data inputs, A through H, of data shift register U77, and to the control register circuit. The address recognition circuit generates AOCK-N and the asynchronous data transfer control circuit generates TCBE-N. AOCK-N activates gate G7 and TCBE-N presets FFl and FF2. The 1 output of FFl disables gate G2 and enables the set input of FF2. The 0 output of FF2 disables G5. When AOCK-N is removed, G7 is disabled and the low-to-high transition output of G7 clocks the data shift register U77 which loads it with the parallal data.

5-492. After the data register is loaded, the asynchronous data transfer control circuit generates TRST-N. TRST-N resets FF3 and the 0 output of FF3 activates G10 (start bit). The output of G10 activates the TTY driver U10, Q4, and T3 and is inverted by inverter I3 which removes SDAT-N.

5-493. The asynchronous data transfer control circuit then generates TRSE-P and TRSA-N. TRSE-P enables gate G6 and TRSA-N enables the data shift register to shift to the left (D07S-P to DOOS-P). At this time, G5 presents a high to the serial data left shift (SDLS) input of data shift register U77.

5-494. TR07-P from, the clock generator circuit enables G6 and once every seventh of 16 CLCK-P pulses G6 is activated. The output of G6 activates G7 and when TR07-P is removed G6 is disabled which disables G7. The low-to-high transition output of G6 triggers FFl through FF3. FF2 remains set which holds G5 disabled, and FFl is cleared which enables gate G2 and disables the set input of FF2. DOOS-P is routed to the set input of FF3 and if DOOS-P is high, FF3 remains set which holds G10 disabled and a 1 is indicated to the external device (first data bit). If DOOS-P is low, FF3 is cleared which activates G10 and a 0 is indicated to the external device (SDAT-N). The low-to-high transition output of G7 clocks the data shift register U77 which shifts once to the left and one stop bit (the output of G5 high) is shifted into the D07S-P position.. The cycle is repeated and the data shift register U77 is again shifted to the left and the second stop bit is shifted into the data shift register U77. FF2 is cleared (FFl cleared) which activates G5 and G5 presents a low to the SDLS input of data shift register U77.

5-495. The cycle is repeated seven times and the second stop bit will be in the DOOS-P position which enables gate G3 and the set input of FF3. Gates G2 and G4 are activated (DOlS-P through 307S-P are low). G2 and G4 activate G3 which generates DAGN-P. DAGN-P is routed to the asynchronous data transfer control circuit and on the next low-to-high transition output of G6 the data shift register is shifted to the left and the last stop bit is transmitted to the external device. G3 is disabled (DOOS-P goes low) which removes DAGN-P and the asynchronous data transfer control circuit removes, TRSE-P which disables G6 and TRSA-N which prevents the data shift register U77 from shifting. The sequence is repeated to transfer the next data word to the external device.

5-496. With a control word for a read operation stored in the control register circuit, RINS-P, RLOP-P, TWX-N, RLPR-N, and BARL-N are generated. RINS-P enables

G5 and RLOP-P enables G10. TRAC-N, RLPR-N and BARL-N are routed to the data multiplexers U56, U58, U67, and U68.

5-497. The asynchronous data transfer control circuit generates RCBC-N and TRST-N. RCBC-N clears the data shift register U77 and TRST-N resets FF3. The asynchronous data transfer control circuit then generates TRSE-P and TRSA-N. TRSE-P enables G6 and TRSA-N enables the data shift register to shift to the left.

5-498. Serial data from the external device is routed to flip-flop FF4, either directly or via inverter I2. When the start bit of the word from the external device is received, FF4 is cleared which disables G5 and activates G10. G5 presents a high to the SDLS input of data shift register U77 and G10 causes a 0 to be coupled back to the external device.

5-499. The data shift register U77 is clocked which causes it to shift to the left as explained during a write operation and the serial data is loaded into it. When the start bit is in the DOOS-P position (high), the set input of FF3 is enabled. FF3 is set, as explained previously, which generates DSTS-P and the stop bit of the word received causes FF4 to be set which generates RDST-P and RDTR-N. DSTS-P, RDST-P, and RDTR-N are routed to the asynchronous data transfer circuit which removes TRSE-P and TRSA-N.

5-500. When the Serial I/O is addressed to read out data stored in the data shift register, the address recognition circuit causes MPXA-P and MPXB-P to go low and generates BDIN-P. This causes the data multiplexers U56, U58, U67 and U78 to couple 1CO and 2CO inputs, DOOS-P through D07S-P, and the 1Y and 2Y outputs, DDOO-N through DD07-N. BDIN-P strobes data bus driver/receivers which couples DDOO-N through DDO7-N to the INFIBUS as DBOO-N through DB07-N, respectively.

5-501. SERIAL I/O CONTROL GROUP ASYNCHRONOUS DATA TRANSFER CONTROL CIRCUIT.

5-502. General. The Serial I/O control group asynchronous data transfer control circuit controls the transferring of data to or from the external device. Control words from the control register circuit enable the asynchronous data transfer control circuit to perform write or read operations. In a write operation, the asynchronous data transfer control circuit controls the conversion of parallel data in the data selector/control circuit to serial data for transmission to the external device. In a read operation, the asynchronous data transfer control circuit controls the conversion of serial data from an external device to parallel data to be stored in the data selector/control circuit.

5-503. Detail Analysis (see figure 70). When the master reset pulse is generated on the INFIBUS or when the status register is written, the control register circuit generates RNIN-N and TNOT-N. RNIN-N resets flip-flops FFl, FF2, FF4, FF5, and activates gate G13 which resets flip-flop FF3. TNOT-N presets flip-flop FF6 and resets flip-flops FF7 and FF8. The 1 output of FF6 enables gate G8.

5-504. With a write operation control word stored in the control register circuit, RNIN-N, TOTR-N and TOTS-P are generated. RNIN-N holds FFl through FF5 reset. TOTR-N activates gate G4 which enables the binary counter U42 to be triggered by CLCK-P from the clock generator circuit and TOTS-P enables gate G14. With TNOT-N high, the preset input of FF6 and reset inputs of FF7 and FF8 are disabled.

5-505. When the external device is ready to accept data, the control register circuit generates TOAK-P which activates G8. G8 generates BTRQ-N to the data selector/control circuit and to the INFIBUS access circuit which generates an interrupt request.

5-506. The binary counter U42 is a divide by 16 counter which counts every high-to-low transition of CLCK-P from the clock generator circuit. It provides a 4-bit binary-coded-decimal number to the 6 and 7 decoder U21 and U51. On the sixth count (0110), the 6 and 7 decoder U21 and U51 6 output enables gates G5 and G6 and on the seventh count (0111), the 6 and

7 decoder generates TR07-P. TR07-P enables gates G7, G14 and G16 and is also routed to the data selector/control circuit.

5-507. When the interrupt is serviced and the serial I/O is slaved and provided with data, the address recognition circuit generates AOCK-N which is coupled through driver DRl. DRl generates TCBE-N which resets FF6 and is routed to the data selector/control circuit which generates the stop bits.

5-508. The 1 output of FF6 (low) disables G8 and the 0 output of FF6 enables G16. When TR07-P is generated by the 6 and 7 decoder U21 and U51, TR07-P activates G16 which enables the set input of FF7. On the next high-to-low transition of CLCK-P, FF7 is triggered and set. The 1 output of FF7 enables its own clear input and the set input of FF8. The 0 output of FF7 activates gates G3 and G15. G3 generates TRST-N which is routed to the data selector/control circuit. G15 generates TSFT-P which is routed to the address recognition circuit.

5-509. On the next high-to-low transition of CLCK-P, FF7 is cleared and FF8 is set. The 0 output of FF7 disables G3 and Gl5. FF8 generates TSER-N which holds G15 activated, disables G16, and activates G17. G17 generates TRSE-P which is inverted by inverter I2 generating TRSA-N. TSER-N and TSFT-P are routed to the address recognition circuit to prevent data from being loaded into the Serial I/O data register. TRSA-N and TRSE-P are routed to the data selector/control circuit to enable data to be serially transmitted to the external device.

5-510. Every TR07-P generated to the data selector/control circuit by the 6 and 7 decoder U21 and U51 causes one data bit to be transmitted to the external device. When the complete word is transmitted, the data selector/control circuit generates DAGN-P which enables G14. The next TR07-P pulse activates G14 which enables the set input of FF6 and clear input of FF8. On the next high-to-low transition of CLCK-P, FF6 is set and FF8 is cleared. The 1 output of FF6 activates G8 which, again, generate:, BTRQ-N to the INFIBUS access circuit for the generation of an interrupt request for the next data word. Also, the data selector control circuit removes DAGN-P which disables G14.

5-511. The cycle of transferring the next word to the external device is repeated as discussed. When all data words required are transferred to the external device, the control register circuit removes TOAK-P which disables G8, preventing interrupt requests from being generated.

5-512. Prior to loading the control register of the Serial I/O for a read operation, the particular Serial I/O is cleared as explained previously. This causes the data selector/control circuit to generate DSTS-P which enables G6.

5-513. With a read operation control word stored in the control register circuit, the control register circuit generates TNOT-N and RINS-P. TNOT-N presets FF6 and resets FF7 and FF8. RINS-P enables gates G8, G9, G11 and activates Gl. The 1 output of FF6 enables G8 and the output of Gl enables the set input of FFl.

5-514. On the high-to-low transitron of CLCK-P, FFl is triggered and set. The 1 output of the FFl enables G5 and the 0 output of FFl activates G4. The output of G4 enables the binary counter U42 to count the high-to-low level transitions of CLCK-P. On the sixth count (0110) the binary counter U42 causes the 6 output of the 6 and 7 decoder U21 and U51 to go high which activates G5 and G5. The output of G5 and CLCK-P activates gate G2. The output of G2 enables G10 and is inverted by inverter I1 which generates RCBC-N. RCBC-N activates G3 which generates TRST-N. RCBC-N and TRST-N are routed to the data selector/control circuit to clear the data register and start bit flip-f lop. This causes the data selector/control circuit to remove DSTS-P which disables G6,.

5-515. On the next high-to-low transition of CLCK-P, FF2 is set and the 0 output of FF2 disables G5 and G7 and activities G17.

The output of G17, TRSE-P, is inverted by I2 which generates TRSA-N. TRSE-P and TRSA-N are routed to the data selector/control circuit to enable the Serial I/O data register to be serially loaded with data from the external device.

5-516. With the set and clear inputs of FF2 both low, FF2 remains set with further high to low transitions of CLCK-P. Every seventh count of CLCK-P by the 4-bit binary counter causes the 6 and 7 decoder U21 and U51 to generate TRO7-P. TR07-P is routed to the data selector/control circuit and one data bit from the external device is loaded into the data register.

5-517. When the entire word is loaded, the start bit of the word causes the data selector/control circuit to generate DSTS-P which enables G6. Also at the same time, the stop bits of the word cause the data selector/control circuit to generate RDTR-N and RDTS-P. RDTR-N disables Gl, G5, and RDTS-P enables G9.

5-518. On the next sixth count by the binary counter U42, the 6 output of the 6 and 7 decoder U21 and U51 activates G6 which enables the clear input of FF2 and activates G9. The output of G9 enables the set input of FF3 and on the next high-to-low transition of CLCK-P, FF2 is cleared and FF3 is set. The 0 output of FF2 enables G7 and the 1 output of FF3 enables G10 and activates G8. G8 generates BTRQ-N which is routed to the INFIBUS access circuit causing an interrupt request to be generated to have the data word read out of the Serial I/O. On the next count (seventh) by the binary decoder U42, the 6 and 7 decoder U21 and U51 generates TR07-P which activates G7. The output of G7 enables the clear input of FFl. On the next high-to-low transition of CLCK-P, FFl is cleared and G4 and G5 are disabled. The high output of G4 prevents the binary counter U42 from counting. When the Serial I/O is slaved to read out the data word, the address recognition circuit generates RCBA-N. RCBA-N activates G13 which resets FF3.

5-519. If the stop bits of the word from the external device are not present, RDTR-N is high which enables G11 and RDTS-P is low which disables G9. When G6 is activated, as explained previously, G11 is activated which enables the set input of FF5. On the next high-to-low transition of CLCK-P, FF5 is set which generates RFER-N. RFER-N activates G12 which generates EROR-N. EROR-N is routed to the INFIBUS access circuit, causing it to generate a format error interrupt request.

5-520. If the data word is not read out of the Serial I/O data register, the address recognition circuit does not generate RCBA-N and FF3 remains set which enables G10. When the next word is being received from the external device, G2 is activated, as explained previously, which activates G10. The previous data word is destroyed and G10 triggers and sets FF4 which generates RQRR-N. RORR-N is routed to the data selector/control circuit. RORR-N also activates G12 which generates EROR-N. EROR-N is routed to the INFIBUS access circuit causing it to generate an overrun interrupt request.

5-521. BLOCK TRANSFER ADAPTER A1A3A13 CONTROL CIRCUIT.

5-522. General. The Block Transfer Adapter (BTA) control circuit recognizes the address and selects the BTA internal registers for reading or writing. It performs direct data transfers (DDT) transferring blocks of data to or from the Core Memory or other Processor functions and slaves the Mag Tape Controller to transfer data to or from the Formatter. The BTA and the Mag Tape Controller are initialized (registers loaded) simultaneously under CPU control and afterwards the BTA becomes the master. When initialized for a write operation, the Formatter indicates ready status to the Mag Tape Controller and the Mag Tape Controller indicates to the BTA to start transfers. When completed, the BTA notifies the Mag Tape Controller to initiate a level 3 interrupt to indicate a completion of a block transfer to the CPU. When initialized for a read operation a similar sequence occurs.

5-523. Detail Analysis (see figure 71). When master reset, MRES-N, is generated

on the INFIBUS, driver DR3 is activated and its output activates gate G14. G14 generates ACIA-N which resets flip-flops FF3 through FF6, FF8, FF10, FF11, FF12 via gate G34, FF14 via gate G37, FF15 via gate G39, and FF16 through FF19.

5-524. For address recognition, the address comparators U9, U17, and U18 compare the jumper encoded address of Jl with the address bits AO3A-P through Al5A-P from the BTA address, data and block length register circuit. A12A-P through AlSA-P are always high for a Processor function address and the output of gate G12 is high. If there is address recognition, the outputs of the address comparators are high which places a high at the set input of flip-flop FFl. Address bits A0lA-P and A02A-P from the BTA address, data and block length circuit are decoded to select the BTA internal registers. To select the status register, A0lA-P and A02A-P are low and the outputs of inverters I9 and I10 enable gate G13. Also the outputs of I9 and I10 activate gate G11 which disables gate G7 and places a low at the set input of flip-flop FF2. To select the control register, AOIA-P and A02A-P are high which enables gate G10 and G11 is again activated. To select the address register, A0lA-P is high and A02A-P is low. AOlA-P and the output of I9 enables gate G9 and G11 is not activated which enables G7 and places a high on the set input of FF2. To select the block length register, A0lA-P is low and A02A-P is high. A02A-P and the output of I10 enable gate G8 and G11 is not activated.

5-525. To write into any of the internal registers, RITE-N (waveform B, figure 72 is generated on the INFIBUS and inverter I6 inverts RITE-N which enables gate G3. To read any of the internal registers, RITE-N is high and the output of I6 is inverted by inverter I7 which enables gates G5 and G7.

5-526. When the BTA status register IS written into, the address is placed on the INFIBUS and RITE-N is generated by the Processor master function. Address recognition takes place and G10 and G13 are enabled. The Processor master function generates STRB-N and inverter I18 inverts STRB-N (waveform C, figure 72) which generates STRA-P (waveform D, figure 72). STRA-P is coupled through drivers DR1 and DR2 and inverter I8 inverts the output of DR2 which triggers and sets FFl. The 1 output (high) of FFl activates gate G1 which activates G3. Inverter I1 inverts the output of G1 and the output of I1 is delayed by delay DL2 for 50 nsec. Then, inverter I2 inverts the output of DL2 and the output of I2 is inverted by inverter I3 which disables G3. The output of G3 activates G13 which activates G14, generating ACLA-N (waveform G, figure 72) which resets the BTA control circuits as explained previously.

5-527. To read the status register, the Processor master function generates the address and does not generate RITE-N (waveform B, figure 73) on the INFIBUS. Address recognition occurs and G5 is enabled and G7 is disabled as explained previously. The Processor master function generates STRB-N and STRA-P (waveform D, figure 73) enables G5. FFl is set and the 1 output, AMAS-F, of FFl activates G5 which generates ASTB-F (waveform E, figure 73). ASTB-P strobes the status data onto the INFIBUS.

5-528. To load the address register within the BTA address, data and block length register circuit, the Processor master function generates the address, data and RITE-N on the INFIBUS. Address recognition occurs and G9 is enabled and G11 is not activated which enables the set input of FF2. The Processor master function generates STRB-N on the INFIBUS and STRA-P sets FFl. F11 generates AMAR-N (waveform F, figure 75 which is routed to the BTA address, data and block length register circuit to enable the address register to be loaded. G9 is activated by the output of G3 and G9 generates ALDA-N (waveform G, figure 75) which activates gate G42. G42 generates CCKA-N (waveform F-I, figure 75) which is routed to the BTA address, data and block length register circuit to load the address register-with the starting address that is on the INFIBUS data lines. FF.2 is triggered and set by the output of I2 and the 1 output (high) of FF2 enables gate G2. I3 disables G3 and after the 50 nssec delay of delay DLl,

I4 activates G2 which generates ADUN-N (waveform I, figure 75). ADUN-N is coupled through driver DRS which generates DONE-N (waveform J, figure 75). The output of I5 is delayed by delay DL3 for 50 nsec which then disables G2, removing DONE-N. To read the contents of the address register, the Processor master function generates the address and RITE-N remains high. G5 and G7 are both enabled by the output of I7 and G11. When FFl is set, AMAS-P activates G5 and G7 generating ASTB-P and ASTA-P, respectively, to the BTA address, data and block length register circuit to strobe the address register contents to the INFIBUS data lines and DONE-N is generated as explained previously.

5-529. To load the block length register within the BTA address, data and block length register circuit, the Processor master function places the address, data and RITE-N on the INFIBUS. G3 and G8 are enabled and address recognition takes place, G3 is activated which activates G8, generating ALDB-N (waveform G, figure 74) to the BTA address, data and block length register circuit. This action loads the block length register with the data from the INFIBUS data lines. FF2 is triggered and set by the output of I2 and the 1 output of FF2 enables G2, I4 activates G2 which generates ADUN-N (waveform H, figure 74). ADUN-N is coupled through DR.5 which generates DONE-N (waveform I, figure 74) and after the 50 nsec delay of DL3, G2 is disabled and DONE-N is removed. To read the contents of the block length register, the Processor master function generates the address and RITE-N remains high. G5 and G7 are enabled by the output of I7 and G11. When FFl is set, G5 and G7 are activated which generates ASTB-P and ASTA-P to the BTA address, data and block length register circuit which strobes the block length register data to the INFlBUS data lines and DONE-N is generated, as explained previously.

5-530. To load the control register, the Processor master function generates the address, control word, and RITE-N. Address recognition takes place and G10 is enabled as explained previously. G3 is activated and its output activates G10 which generates ACNT-P (waveform G, figure 76). Inverter Ill inverts ACNT-N which generates ACWT-N (waveform H, figure 76). At this time, the BTA address, data, and block length register circuit is presenting the control word bits DOOA-P, DOlA-P and D07A-P to the control register flip-flops FF8, FF9, and FF11, respectively. The leading edge of ACNT-P triggers FF11, loading it with D07A-P and on the trailing edge of ACNT-P FF9 is triggered, loading it with DOOA-P. The 0 output (low) of FF9 activates gate G32. On the trailing edge of ACWT-N, FF8 is triggered loading it with DOlA-P. On the trailing edge of AMAS-P (waveform F, figure 76), FF9 is cleared and G32 is disabled. The high-to low transition output of G32 triggers flip-flops FF12 and FF 14. If the block length register is loaded, LAZE-N from the BTA address, data, and block length register circuit is high which enables the set input of FF14. FF14 is set by the high-to-low transition output of G32 and the 1 output (high) of FF14 enables gate G36. The 1 output (high) of FF11 enables gate G31 and activates G36 which enables gate G35. The 0 output of FF11, ABAR-N, is routed to the BTA address, data and block length register circuit. To write the block length register, DOlA-P is high and FF8 is set. The 1 output, AMDS-P, of FF8 enables gate G30 and disables gate G4. The 0 output, AMDR-N, of FF8 disables G30 and is also routed to the BTA address, data and block length register circuit. For a read operation DOlA-P is low and FF8 is not set. AMDS-P (low) disables G30 and enables G4. The Mag Tape Controller cycles, loading its control register and then generates DONE-N on the INFIBUS. To read the control register contents, the cycle is repeated as explained previously for reading the status register, but the BTA address, data and block length register circuits strobe the control data to the INFIBUS.

5-531. The Mag Tape Controller will generate a request for data when instructed by the Formatter and BTBl-N (waveform A, figure 77) will be received (BTAl-N from the Mag Tape Controller). Inverter I21 inverts BTBl-N activating gate G35 (FF11 and

FF14 set) which generates CCSN-P (waveform B, figure 77). If the INFIBUS is not busy, SELD-N will be high which enables gate G18. As CCSN-P is generated G18 will be activated. The output of G18 sets FF3. The 1 output of FF3, enables gates G16 and G19 and activates gate G15. The output of G15 is coupled through driver DR4. The output of DR4, SRLD-N (waveform C, figure 77) is the highest priority infibus access request and the Bus Controller detects this request and responds with SELD-N (waveform D, figure 77) and PCDA-P (waveform E, figure 77). SELD-N disables G18 and is also inverted by inverter I12 which enables G19 and activates G16. With G16 activated, G17 is disabled and PCDB-P is not generated. PCDA-P activates G19 which sets FF4 and disables gate G21. The 1 output of FF4 activates gate G20 and enables G21. The 0 output of FF4 disables G18 and G15 and activates driver DR3 which generates SACK-N (waveform P, figure 77). Disabling G15 causes SRLD-N to return to high. The Bus Controller then removes PCDA-P and G19 is disabled which activates G21. G21 resets FF3 and G15 and G16 will be disabled by the 1 output of FF3 (low). With G16 disabled, G17 is once again enabled to generate PCDB-P. SELD-N is then removed by the Bus Controller which enables G18 and it is also inverted by I12 which disables G16 and G19. At the same time, the 1 output (high) of FF4 activates gate G20. The output of G20 sets FF5 and activates gate G24. BOLA-P (waveform G, figure 77) is generated by G24 -which is routed to the BTA address, data and block length register circuit to strobe the first address of the address register to the INFIBUS (waveform l-l, figure 77). BOLA-P does not activate G4 because AMOS-P is being generated for a write operation (presenting data to the Formatter), disabling G4. BOLA-P also activates G43 which generates BYTE-N (waveform I, figure 77). G25 is also enabled by BOLA-P and will is activated if the transfer is not completed within 2 usec. In this cycle, data is to be read out of the Core Memory and RITE-N is high. The address is generated and the Core Memory will present the data (from address selected) on the INFIBUS data lines.

5-532. The Bus Controller will generate QUIT-N if the transfer is not completed within 2 usec. Inverter I16 inverts QUIT-N which activates gate G25. G25 sets FF7 which generates BABR-N which triggers and sets FF13. The output of FF13 activates gate G33 which activates gate G31. The output of G31, BT4B-N, causes the Mag Tape Controller to generate a level 3 interrupt request. This halts the current operation and the CPU tests status to initiate the operation once again.

5-533. In a normal cycle (within 2 usec), BOLA-P enables G28 and BOLA-P is also inverted by inverter I15. After the 50 nsec delay of delay DL4, G28 is activated by the output of I15 which generates STRB-N (waveform K, figure 77). With the strobe (STRB-N) generated, the Core Memory will generate the data from the address generated by the BTA. It will take approximately 325 nsec for the Core Memory to place the data on the INFIBUS data lines. As STRB-N is generated, inverter I18 inverts STRB-N and generates STRA-P (waveform L, figure 77) which activates G22, clearing FF4. Inverter I13 also inverts STRA-P, disabling G20. At the same time, the 0 output (low) of FF5 disables G18 and the 1 output (high) enables G26 and activates G27. G27 activates G24 and the output of G27 is also routed to the INFIBUS as BTB2-N (waveform J, figure 77). BTB2-N notifies the Mag Tape Controller to accept the data present on the INFIBUS data lines and present it to the Formatter. BTB2-N (BOND-N) also activates G37 which resets FF14. The 1 output (low) of FF14 disables G36 which disables G35, removing CCSN-P.

5-534. The Core Memory, having receiving an address with the RITE-N line high (read), **will** generate the data from the address specified. After the dats is stabilized on the INFIBUS data lines, the Core Memory Controller generates DONE-N **(waveform** N, figure 77). inverter I19 inverts DONE-N generating BDNA-P (waveform 0, figure 77) which activates G27 and G26. Inverter I14 inverts BDNA-P, disabling G20 and G23. The output of G26 sets FF6 and the 1 output (high) of FF6 enables G23. The Mag Tape

Controller also receives DONE-N and strobes the data from the INFIBUS data lines into its output data register, presenting the data to the Formatter. As BDNA-P is generated, FF15 is set because BOLA-P is being generated at this time, which enables the set input. G38 is activated by the 0 output of FF15 which presets FF19. CEXR-N (waveform S, figure 77), is generated by FFl9 and **disables** G1. On the trailing edge of BDNA-P, G26 and G27 are disabled. I14 now activates G23, which clears FF5. The 0 output of FF5 enables G18 and the 1 output of FF5 disables G27, G22 and G26 and resets FF6. The output of G27 now disables G24, G28 and G44. G28 removes STRB-N and G44 removes BYTE-N. With STRB-N removed STRA-P is also removed which disables G22 and I13 once again enables G20.

5-535. When CEXR-N is generated by FF19, FFl5 is set. I22 inverts CLKA-N (waveform Q, figure 77) and FF16 will be set on the next high-to-low transition of the output of I29. The 1 output of FF16 enables its own clear input and the set input of FF17. Also, gares G40 and G41 are activated because LAZE-N is only generated when the block **length** register is at zero (all transfers completed) and AFXA-N is only generated when the address register is fully incremented (the required addresses completed). The output of G40, CDEC-N (waveform U, figure 77), decrements the block length register and the output of G41 activates G42 which generates CCKA-N (waveform V, figure 77). CCKA-N clocks (increments) the address register. At the same time, the 0 output of FF16 activates G39 which clears FF15. On the next high-to-low transition output of I22, FF16 is cleared and FF17 is set. G40, G41, and G42 are disabled, which removes CDEC-N and CCKA-N. On the next nigh-to-low transition output of I22, FF17 is cleared and FF18 is set. FF18 generates CX3R-N (waveform Y, figure 77) which activates gate G32 and on the next high-to-low transition output of I22, FF18 clears which removes CX3R-N. The low-to-high transition of CEXR-N clears FFl9 and also disables G32. FF12 *and* FF14 are clocked by the high-to-low output transition of G32 and if the block length register is at zero (LAZD-P high and LAZE-N low), FF12 will set. If the block length register is not at zero, LAZD-P is low and LAZE-N is high and FF14 is set.

5-536. If there is to be another transfer (the block transfer not completed), LAZE-N input is high and only FF14 will be set. With FF11 enabling G36, the 1 output of FF14 activates G36 which enables G35. When the Formatter notifies the Mag Tape Controller to perform another transfer, BTBl-N is again received and inverted by I21. This activates G35 which generates CCSN-P and the entire sequence is repeated for the next data word to be written.

5-537. When all the transfers are completed, LAZD-P and LAZE-N are generated and as FF12 and FF14 are clocked, only FF12 is set. The 0 output (low) of FF12, CBLR-N, is routed to the BTA address, data and block length register circuit to be placed in the seventh bit position of the data word when the status register is read to indicate the completion of transfers. The 1 output of FF12 enables G29 and G31. On the next request G29 (BTBl-N) is activated which activates G30. The output of G30 activates G33 which activates G31. G31 generates BTB4-N (waveform Z, figure 77) which is a request to the Mag Tape Controller to generate a level 3 interrupt to indicate to the CPU that the entire block of data words has been transferred.

5-538. If after or during the write operation, a timing error occurs in the Mag Tape Controller, BTB3-N will be generated which indicates an error condition. I20 inverts BTB3-N which triggers and sets FF10. The output of FF10 disables G35 and activates G33. The output of G33 activates G31 which generates BTB4-N, as explained previously.

5-539. During read operation of the Formatter, operation is similar to a write operation. When loading the control register, the l-bit position (DO1A-P) will be low and FF8 is not set. The 0 output (high) of FF8 enables G30 and when the specified number of transfers are completed, FF12 is set, as explained

previously. The 1 output of FF12 activates G29 which activates G30 and BTB4-B is generated, as explained previously.

5-540. BLOCK-TRANSFER ADAPTER A1A3A13 ADDRESS, DATA, AND BLOCK LENGTH CIRCUIT.

5-541. General. The Block Transfer Adapter (BTA) address, data, and block length circuit consists of the address bus driver receivers, address register, block length register, data bus driver receivers, and data multiplexer. Address data is received or transmitted by the address bus driver receivers and the address register holds the Core Memory address to or from which data is to be transferred or device address (device number). The number of data transfers to be performed is stored in the block length register and the data to be transferred to or from the INFIBUS data lines is first selected by the data multiplexer then strobed to the INFIBUS via the data bus driver receivers. This circuit also generates increasing addresses. Each transfer of data to or from Core Memory increases the address and decreases the block length by one. When the maximum address or zero block length is reached, the transfers stop.

5-542. Detail Analysis (see figure 78). The address bus driver receivers U10, U19, U20, and U30 transmit and receive the 16-bit address. (AB00-N through ABl5-N). Address bits ABOl-N through ABl5-N are inverted by address bus driver receivers Ul0, U19, U20, and U30 (inverter I1) generating AOlA-P through Al5A-P. The O-bit position is not an input to the BTA. AOlA-P through Al5A-P are routed to the BTA control circuits for address (device number) recognition. AOlA-P and A02A-P are also applied to the select inputs of the data multiplexers U58, U66 and U67, U68, and U79. In a read cycle of the BTA contents, the address recognition logic receives the address for recognition and at the same time the data multiplexers will select the data to be placed on INFIBUS data lines as determined by the levels of AOlA-P and A02A-P.

5-543. Address data, AOOB-N through Al5B-P, stored in the address register/counters U53, U64, U65, and U76 are inverted by inverters I2 through I17 and is applied to address bus driver receivers U10, Ul9, U20, and U30. BOLA-P from the BTA control circuits strobes address bus driver receivers UlO, U19, U20, and U30 when information is to be transferred to the INFIBUS, generating ABOl-N through ABl5-N as determined by the data (or count) in address register/counters U53, U64, U65, and U76.

5-544. When the starting address is on the INFIBUS data lines DBOO-N through DBl5-N are coupled through the data bus driver receivers generating DOOA-P through Dl5A-P. AMAR-N goes low, parallel loading address register counters U53, U64, U65 and U76 with the number determined by DOOA-P through Dl5A-P. For each transfer of data to or from the Core Memory, CCKA-N is generated by the BTA control circuits and is applied to the clock inputs of the four address registers/counters. Address register/counter U65 is clocked and counts 0 to 15, generating its carry output on the fifteenth count. The carry output of address register/counter U65 clocks U64 to count 1 on the sixteenth CCKA-N input and address register/counter U65 resets to zero. This cycle repeats itself until address register/counters U64 and U65 are both fully loaded (count equals 256, the carry outputs of address register/counters U64 and U65 enable address register counter U53 to count 1. This cycle repeats itself until address register/counters U53, U64, and U65 are fully loaded (count equals 4096). The carry outputs of address register counters U53, U64, and U65 will be generated enabling U76 to count 1. The cycle repeats itself until all four address register/counters are fully loaded (count equals 65, 536). With address register/counter U76 fully loaded (all outputs high), 62 is activated generating AFXA-N which is routed to the BTA control circuits. AFXA-N prevents the BTA control circuits from generating any more CCKA-N clock pulses. There is one CCKA-N input for each byte transfer.

5-545. When the data on the INFIBUS data lines is the block length (number of words to be transferred to or from the Core Memor-y), ALDB-N goes low parallel loading block length registers/counters U54, U62, U63, and U76 with the number determined by DOOA-P through Dl5A-P. Block register/counters U54, U62, U63, and U77 operation is similar to the address register/counters U53, U64, U65, and U76, except they count down and the MIN output enables the next block length register counter. The outputs of block length register/counters U54, U62, U63, and U77 are inverted by inverters I18 through I34 generating LOOA-N through Ll5A-N which are applied to data multiplexers U56, U66, U67, U68 and U79 for selection. U62 is always enabled and CDEC-N clocks all four counters simultaneously. On the first 16 CDEC-N inputs block length register/counter U62 will decrement from 15 to 0 (binary) and on the 0 count, the MIN (minimum) output of U62 will go high. I26 inverts this output which enables U63 to decrement once on the next CDEC-N input. The cycle will be repeated until block length register/counters U62 and U63 are decremented to 0 and both of their MIN outputs will be high. G4 is now activated which enables block length register/counter U54 to decrement on the next CDEC-N input. The cycle will be repeated until block length register/counters U54, U62, and U63 are at 0 and the MIN outputs are high activating G3. G3 enables block length register/counter U77 to decrement once on the next CDEC-N input. Again, the entire cycle will be repeated until all four block length register/counters are at 0 and the MIN outputs are high activating G5. The output of LAZE-N, is routed to the BTA control circuit indicating the block length register has decremented to zero. I35 inverts LAZE-N generating LAZD-P which is routed to the BTA control circuit. These outputs notify the BTA control circuit that the entire block of **data** transfers has been completed.

5-546. Data multiplexers U56, U66, U67, U68, and **U79** select data from the block length register (LOOA-N through Ll5A-N), address register (A00B-N through Al5B-N), status register BTA control circuit ABTR-N and CLBR-N), or control register (BTA control circuit ABAR-N and AMDR-N).

5-547. When the **status** register is to be read out of the BTA onto the INFIBUS data lines, A02A-P and AOlA-P will be low which couples CBLR-N to M07X-N, ABTR-N to MOGX-N and 5 volts to MOlX-N. Also, MOOX-N, MOlX-N, MOGX-N, and M07X-N are routed to bus driver receiver U69. After address recognition by the BTA control circuit, ASTB-P is generated and strobes data bus driver receiver U69 which generates DBOO-N, DBOl-N, DBO6-N, and DB07-N. At the same time data multiplexers U56, U68 and U79 select the address register data (A02B-N through AO5B-N and A08B-N through A15B-N) and M02X-N through M05X-N and M08X-N through Ml5X-N are routed to data bus driver receivers U6O, U70 and U80, but will not be strobed onto the INPIBUS data lines because ASTA-P is not generated.

5-548. To read out the control register contents of the BTA, operation is similar to when the status register is read, except A0lA-P and A02A-P are high which couples ABAR-N to M07X-N, 5 volts to M06X-N, AMDR-N to MOlX-N, and 5 volts to MOOX-N bit posit ion. They are routed to data bus driver receiver U69 and strobed to the INFIBUS data lines by ASTB-P. At the same time, data multiplexers U56, U68 and U79 select the block length register data (L02A-N through LO5A-N and L08A-N through L15A-N), but this data is not strobed out because ASTA-P is not generated.

5-549. To read out the block length register data (LOOA-N through L15A-N), AOlA-P is low and A02A-P is high and LOOA-N through L15A-N are coupled through data multiplexers U58, U66, U67, U68, and U79 which generate MOOX-N through M15X-P. ASTB-P strobes bus driver/receiver U69 and ASTA-P strobes bus driver/receivers U60, U70, and U80 which generate DBOO-N through DB15-N. LOOA-P through L15A-P determine the levels of DBOO-N through DB15-N.

5-550. To read **out** the address register data (AOOB-N through A15B-N), A02A-P is low and A0lA-P is high. Data multiplexers U66

and U67 select the address register data (AOOA-N, A0lA-N, AO6A-N and A07A-N) and data multiplexers U56, U68 and U79 select the address register data (A02A-N through AO5A-N and A08A-N through A15A-N). MOOX-N through M15X-N are generated as determined by the levels of AOOA-N through A15A-N and routed to data bus driver/ receivers U60, U69, U70, and U80. ASTA-P strobes data bus driver receivers U60, U70 and U80. ASTB-P strobes data bus driver receiver U69 which generates DBOO-N through DB15-N.

5-551. MAG TAPE CONTROLLER A1A3A14 ADDRESS RECEIVERS AND RECOGNITION CIRCUIT.

5-552. General. The Mag Tape Controller address receivers and recognition circuits recognizes the Mag Tape Controller address when being slaved by a master function. It selects the internal registers of the Mag Tape Controller and performs a read or write operation as determined by the master function slaving the Mag Tape Controller.

5-553. Detail Analysis (see figure 79). The device number connector J3 connections determine the Mag Tape Controller address (device number). DN04-N through DN11 -N, device number bits, are routed to the Mag Tape Controller data input and selector circuit to be placed on the INFIBUS data lines when the Mag Tape Controller is requesting a level 3 INFIBUS access. The device number inverters (19 shown) generate DA04-P through DA11-P. ABOl-N through AB15-N from the INFIBUS address lines are inverted by address bus receivers U10, U20, U29, and U40 (11 shown) which generate AOlA-P through A15A-P .

5-554. A04A-P through A11A-P are applied to the address recognition gates U19, U28, and U39 (Gl shown) where they are compared with the jumper encoded device number (DA04-P through DA11-P). If there is a match at the inputs, the corresponding outputs of the address recognition gates U19, U28, and U39 will be high. Also, for address recognition, A12A-P must be high which is coupled through driver DRl. In addition A13A-P, A13A-P and A15A-P must be high which activates Gate G2. The combined outputs of the address recognition gates U19, U28, and U39, DRl, and G2 will be high which places a high at the set input of flip-flop FFl.

5-555. Inverters I2, I3, and I5, and gates G3 through G6 decode AOlA-P, A02A-P, and A03A-P to select the control, status, or data registers in the Mag Tape Controller data output and control register circuits. To select the control register, AOlA-P and A02A-P are high and A03A-P is low. Gate G4 is enabled by AOlA-P and A02A-P and the high output of I5. G4 is activated and generates ACNT-N when FFl is set. To select the status register, AOlA-P, A02A-P and A03A-P are all low and the high outputs of I2, I3, and I7 enable G5. When FFl sets, G5 is activated which generates AWST-N. To select the data register, AOlA-P and A02A-P are low and A03A-P is high. G6 is enabled by the outputs of I2 and I3, and A02A-P. When FFl is set, G6 will be activated which generates ADAT-P. Gate G7 will be disabled if the correct combination of AOlA-P, A02A-P and A03A-P are received to select one of the Mag Tape Controller internal registers.

5-556. When data is to be loaded into the Mag Tape Controller data register, the master function generates the address (waveform A, figure 42), data, strobe and RITE-N (waveform B, figure 42) on the INFIBUS. The address will be recognized which enables FFl to be set as explained previously. G3 generates AABL-P (waveform C, figure 42) and enables the set input of flip-flop FF2. RITE-N is inverted by inverter I11 which enables G7 and G10. The output of I11 is also inverted by inverter I12 which disables gate G11 and ARED-P goes low. If the Formatter is ready to accept data, WBAR-N IS low which disables gate G7. The high output of G7 enables gate G8. The Mag Tape Controller INFIBUS access circuit generates STRA-P (waveform D, figure 42) which IS coupled through driver DR2. The output DR2 is coupled through driver DR3 then delayed 50 nsec by delay DL4. The output of DL4 activates gate G8 which triggers and sets FF1. If the Formmatter is not ready

to accept data, WBAR-N from the read-write control status circuit is high which activates G7. The output of G7 now disables G8 until the Formatter is ready. When ready, WBAR-N returns to low disabling G7 which activates G8.

5-557. The output of FF1, AMAS-P (waveform E, figure 42), activates G6 which generates ADAT-P (waveform F, figure 42). Inverter I6 also inverts AMAS-P and the output of I6 is delayed 50 nsec by delay DL1. After the delay, inverter I7 triggers and sets FF2 which enables gate G9. The output of I7 also activates gate G10 which generates AWRT-P (waveform G, figure 42). AWRT-P loads the data register in the Mag Tape Controller data output and control register circuits. The output of I7 is also inverted by inverter I8 and the output of I8 is delayed 50 nsec by delay DL2. After the delay, G10 is disabled and the output of I8 is inverted by inserter I9 which activates gate G9. G9 generates ADUN-N (waveform H, figure 42) which causes the May Tape Controller INFIBUS access circuit to generate DONE-N which indicates a completed data transfer. Inverter I10 then inverts the output of I10 and after the 50 nsec delay of delay DL3, G4 is disabled which removes ADUN-N (high).

5-558. To read the Mag Tape Controller data register, the master function places the Mag Tape Controller address on the address lines and RITE-N will be high. The address is recognized and G6 is enabled and G3 generates AABL-P as explained previously. I11 inverts the high RITE-N input and disables G7 and G10 Inverter I12 inverts the output of I11 and generates ARED-P (waveform A, figure 43) **which** enables **gate** G11.

5-559. The remainder of the cycle of reading the data register is similar to when writing the data register except, when I7 inverts the delayed output of I6, G11 is activated. G11 generates DRBB-N (waveform B, figure 43) and after I9 inverts the delayed output of I8, G9 is activated. I10 inverts the output of I9 which disables G11. 50 nsec later, G9 is disabled and removes ADUN-N.

5-550. The control register write operation is similar to the data register write operation except, G4 is enabled as explained previously and then activated by AMAS-P which generates ACNT-N. ACMT-N activates gate G13 which generates MPXB-P. The control register read operation is similar to the data register read operation, except ACNT-N is generated, G13 is activated, generating MPXB-P which is used by the Mag Tape Controller data input and selector circuit during the read operation to select the control register data to be placed on the INFIBUS data lines.

5-561. The status register write operation; is similar to the other write operations except, G5 is activated. G5 generates AWST-N to the Mag Tape Controller data output and control register circuit which generates a general reset for the Mag Tape Controller function. AWST-N activates gate G12 which generates MPXA-P. The status register read operation is similar to the other read operations except, when AWST-N is generated by G5, G12 is activated. The output of G12, MPXA-P, is routed to the Mag Tape Controller data output and selector circuit to select the status data that is to be placed on the INFIBUS data lines.

5-562, When the Mag Tape Controller INFIBUS access circuit is requesting INFIBUS access, BONE-K is low. BONE-N activates G12 and G13 which generate MPXA-P and MPXB-P, respectively. With MPXA-P and MPXB-P both high the Mag Tape Controller data output and control register circuit generates the Mag Tape Controller device number which is strobed to the INF1BUS data lines.

5-563. Mag TAPE CONTROLLER A1A3A14 INFIBUS ACCESS CIRCUIT.

5-564. General. The Mag Tape Controller INFIBUS access circuit performs the function of obtaining access to the INFIBUS on the assigned interrupt level when data is to be transferred or when an error, while transferring data, has occurred.

5-565. Detail Analysis (see figure 80). When the master reset pulse, MRES-N, is

generated on the INFIBUS or when the Mag Tape Controller is slaved to write into its status register, the Mag Tape Controller data output and control register circuit generates GRSA-N. GRSA-N clears flip-flops FF2 through FF5, and activates gate G13 which resets flip-flop FFl.

5-566. When a control word that enables interrupts is stored in the Mag Tape Controller data output and control register circuit, CR2S-P (waveform A, figure 45) is generated which enables the set input of FFl.

5-567. When the Mag Tape Controller notifies the Block Transfer Adapter to perform a transfer, the Mag Tape Controller read/write control status circuit generates PDSA-N (waveform C, figure 45) which enables gate G5. At the same time, if the Formatter function generates STS2-N, STS2-N activates G5. The output of G5 activates gate G6 and the output of G6 activates gate Gl. Or, if the Formatter function generates SC low, inverter I2 inverts the low SC and the output of I2 activates G6 which activates G1. If an error is detected when transferring data to or from the Formatter function, the Mag Tape Controller read/write control status circuit generates EROR-N (waveform D, figure 45) which activates Gl. When the Block Transfer Adapter completes all required transfers, the Mag Tape Controller data output and control register circuit generates CATS-P (waveform B, figure 45) which activates Gl.

5-568. When any of the cases discussed which activates G1 occurs, the output of Gl is inverted by inverter I1 which triggers and sets FFl. The 1 output of FFl activates gate G7 which sets FF2 and disables gates G2 and G8. The 1 output of FF2 enables G2 and G8, and activates G4. The output of G4 is coupled through driver DRl which generates SRL3-N (waveform E, figure 45).

5-569. The Bus Controller senses SRL3-N and returns SEL3-N (waveform F, figure 45) and the precedance pulse PCDA-P (waveform G, figure 45). SEL3-N disables G7. The output of G7 enables G8 and activates G2 which disables G3. PCDA-P activates G8 and the output of G8 disables G10 and sets FF3. The 0 output of FF3 disables gates G7 and G4. Disabling G4 causes SRL3-N to be removed. The 0 output of FF3 is also coupled through driver DR2 which generates SACK-N (waveform H, figure 45). The Bus Controller senses SACK-N and removes SEL3-N which disables G7. Also, when PCDA-P returns to low, G8 is disabled. This activates G10 and the output of G10 clears FF2. The 1 output (low) of FF2 disables G2, G4 and G8, and the output of G2 enables G3 to couple PCDA-P through to the INFIBUS as PCDB-P. The 1 output of FF3 enables G10, and activates gate G9 which sets FF4 and activates gate G14.

5-570. The 0 output of FF4 disables G7, and the 1 output of FF4 enables gates G11 and G15, and activates G16. G16 generates BONE-N (waveform I, figure 45) which also activates G14. G14 generates BOLA-P (waveform J, figure 45) and BOLA-P and BONE-N cause the Mag Tape Controller device number to be placed on the INFIBUS **data** lines. Also, BOLA-P enables gates G17 and G18, and is inverted by inverter I8. The output of I8 is delayed 50 nsec by delay DLl which then activates G18. G18 generates STRB-N which is routed to the INFIBUS and also Inverted by inverter I9 which generates STRA-P (waveform K, figure 45). STRA-P activates G11 which clears FF3. The 0 output (high) of FF3 enables G4 and G7 and causes SACK-N to be removed. The 1 output of FF3 disables G9 and G10. STRA-P is also inverted by inverter I7 which disables G9.

5-571. After the data is transferred, DONE-N (waveform M, figure 45) is received. DONE-N is inverted by inverter I4 which generates BDNA-P (waveform N, figure 45). BDNA-P activates G15 and G16, and is also inverted by inverter I3. The output of G15 sets FF5 and activates G13 which resets FF1. The output of I3 disables G9 and G12. With FF5 set, Gl2 is enabled and when DONE-N returns to high, BDNA-P goes low which disables G15 and G16 removing BONE-N. The output of I3 now activates G12 which clears FF4. The

output of G16 (high) disables G14 which removes BOLA-P. BOLA-P (low) now disables G18 which removes STRB-N. Clearing FF4 disables G11, G15, and G16, clears FF5, and enables G7.

5-572. If DONE-N is not received within 2 usec after STRB-N goes low, the Bus Controller generates QUIT-N. Inverter I5 inverts QUIT-N which activates G17 (G17 enabled by BOLA-P during the normal cycle}. The output of G17 clears FF3 and FF4, and activates G13 which resets FFl. Inverter I6 inverts the output of I5 which disables G9 to allow G15 to clear FF4.

5-573. MAG TAPE CONTROLLER A1A3A14 DATA INPUT AND SELECTOR CIRCUIT.

5-1574. General. The Mag Tape Controller data input and selector circuit stores data received from the Formatter function. The Mag Tape Controller data input and selector circuit also selects the data to be placed on the INFIBUS.

5-575. Detail Analysis (see figure 81). When the Mag Tape Controller performs a read operation with the Formatter function, the Formatter function generates data, IDOO-P through ID07-P, and IDSB-N ID07-P are routed to input data register U67 and IDSB-N triggers single-shot SSl. SS1 remains set for 3 usec. After 3 usec the 0 output of SSl (waveform B, figure 82) triggers single-shot SS2. SS2 generates RDST-P (waveform C, figure 82) and RDST-N (waveform D, figure 82), for 1 usec. RDST-N triggers and loads input data register U67 with IDOO-P through ID07-P. Also, RDSP-P an:! RDST-K are routed to the May Tape Controller read/write control status circuit. input data registers UG7 and U77 generate RROO-N through RR15-N, and STS5-N through STS8-N which are routed **to data** selectors **M1 through M6 for** selection.

5-576. All data to be placed on true INFIBUS data lines is first selected 'by the data selectors M1 through M6. M1 through M4 are dual four-line to one-line selectors whose output data is determined by the value of MPXA-P and MPXB-P. M5 and M6 are each quad two-line to one-line selectors. The output of M6 is determined by the value of MPXA-P. The output data of M5 is determined by the value of BOLA-P.

5-577. When the Mag Tape Controller is slaved to read the data from the Formatter function, MPXA-P, MPXB-P, and BOLA-P are low. Ml through M4 couple the 1CO and 2C0 inputs to the Yl and Y2 outputs, respectively. M5 and M6 couple the 1A through 4A inputs to the Yl through Y4 outputs, respectively. This condition couples the data from the input data register, RROO-N through RR15-N, to the data output and control register circuit (DOOA-N through DlSA-N).

5-578. When the Mag Tape Controller is slaved to read the Mag Tape Controller control register data from the Mag Tape Controller data output and control register circuit, the Mag Tape Controller address receivers and recognition circuit generates MPXB-P (MPXA-P and BOLA-P low). Ml through M4 couples the lC2 and 2C2 inputs to the Yl and Y2 outputs, respectively. M5 and M6 couple the 1A through 4A inputs to the Yl through Y4 outputs, respectively. This condition couples the control register data, CROO-N through CR05-N, to the Mag Tape Controller data output and control register circuit.

5-579. When the Mag Tape Controller is slaved to read out the status data, the Mag Tape Controller address receivers and recognition circuit generates MPXA-P (MPXB-P and BOLA-P low). Ml through M4 couples the 1C1 and 2C1 inputs to the Yl and Y2 outputs, respectively. M5 couples the 1A through 4A inputs to the Yl through Y4 **outputs,** respectively. This condition **couples the** Maq Tape Controller status data, WDNB-N, RDNA-N, RTER-N, and PDSA-N, and Formatter function status data, NDE-N, DRE-N, STS1-N, and STS2-N to the Mag Tape Controller data output and control register circuit.

5-580. When the device number is to be placed on the INFIBUS data lines during an interrupt request, the Mag Tape Controller address receivers and recognition

circuit generates MPXA-P and MPXB-P, and the Mag Tape Controller INFIBUS access circuit generates BOLA-P. Ml through M4 couples the lC3 and 2C3 input:; to the Yl and Y2 outputs, respectively. M5 couples the 1B through 4B inputs to the Yl through Y4 outputs, respectively. This condition couples the device number, DNO4-N through DN11-N, to the Mag Tape Controller data output and control register circuit.

5-581. MAG TAPE CONTROLLER DATA OUTPUT AND CONTROL REGISTER CIRCUIT.

5-582. Genera 1. The Mag Tape Controller data output and control register circuit stores control words which specify read or write operations. It also stores data which is transferred to the Formatter Function.

5-583. Detail Analysis (see figure 83). When the master reset pulse, MRES-N, is generated on the INFIBUS, inverter I11 inverts MRES-N and the output of Ill activates gate G9 which generates GRSA-N. GRSA-N is inverted by inverter I12 which generates GRSC-P. If the Mag Tape Controller is slaved to write into its status register, the Mag Tape Controller address receiver and recognition circuit generates AWST-N (waveform A, figure 84) and AWRT-P (waveform B, figure 84). AWST-N enables gate G11 and AWRT-P is inverted by inverter I14 which activates G11. The output of G11 activates G9 which generates GRSA-N (waveform C, figure 84) and I12 generates GRSC-P (wave form D, figure 84). GRSA-N resets control register U66 (flip-flop FF2 shown) and also, GRSA-N and GRSC-P are routed to the Mag Tape Controller read/write control status circuit. This causes the Mag Tape Controller read/write control status circuit to generate WBAS-P (waveform E, figure 84) which enables gate G10.

5-584. When the Mag Tape Controller is slaved to read out its status register, the Mag Tape Controller address receiver and recognition circuit gene ates AABL-P (waveform A, figure 85) and ARED-P (waveform B, figure 85) which enables gate G15. The Mag Tape Controller INFIBUS access circuit then generates STRA-P (waveform C, figure 85) which activates G15. The output of G15 enables gates G13, Gl4 and G16. The Mag Tape Controller address receiver and recognition circuit then generates AMAS-P (waveform D, figure 85) and AWST-N (waveform E, figure 85). AMAS-P activates G13 which generates DBRA-P (waveform F, figure 85). RWST-N is inverted by inverter I15 which activates G6 and G16 generates DBRC-P (waveform G, figure 85). At the same time, the Mag Tape Controller data input and selector clrcuit generates DOOA -N through D15A-N (representing status data) which ***are*** routed to the data bus driver/receivers U69, U70, U79, and U80. DBRA-P strobes data bus driver/receivers U70 and U80 which couples DOOA-P through DO5A-N, D08A-N, and DO9A-N to the INFIBUS data lines DBOO-N through DBO5-N, DB08-N, and DB09-N . DBRC-P strobes data bus driver/receivers U79 which couples D12A-N through D15A-K to the INFIBUS data lines. After the transfer is completed, STRA-P is rcmoved which causes the status data to be removed from the INFIBUS.

5-585. When the Mag Tape Controller is slaved to load a control word into its control register, DB00-N through DB05-N (waveform A, figure 86) which represents the control word are on the INFIBUS. DB00-N through DB05-N are inverted by data bus driver/receiver U80 and routed to the inputs of control register U66. The Mag Tape Control address receiver and recognition circuit generates ACNT-N (waveform B, figure 86) which enables gate G12. Afterwards, the Mag Tape Controller address receiver and recognition circuit generates AWRT-P (waveform C, figure 86) which is inverted by I14 and the output of I14 activates G12 which generates WRCO-P (waveform D, figure 86). WRCO-P triggers and loads control register U66 with the control word. Also, WCRO-P is routed to the Mag Tape Controller read write control status circuit.

5-586. If a write control word is presented on the INFIBUS data lines, DB00-N and DB01-N are both low which causes gate G4 to be disabled and gate G7 to be acti-

vated which presents a high to the control register. When the control register is loaded with the control word, CR1S-P is generated which enables G10. Also, CR1S-P is routed to the Mag Tape Controller read/write control status circuit. If a read control word is presented on the INFIBUS data lines, DBOO-N is low and DBOl-N is high which causes G7 to be disabled and G4 to be activated. G4 generates CROA-P for the duration of the loading of the control register cycle. When the control register is loaded with the control word, CROS-P is generated which enables G13, G14 and G16. Also, CROS-P is routed to the Mag Tape Controller read/write control status circuit. In both cases, CR2S-P is generated by control register U66 which is routed to the Mag Tape Controller INFIBUS access circuit to enable interrupts. Gates G2 and inverters I3 through I6, and I8 invert the outputs of the control register and generate CROO-N through CR05-N which are routed to the Mag Tape Controller data input and selector circuit. For a read or a write control word, gates G5 and G8, drivers DR2 and DR3, and inverters I9 and I10 decode the outputs of control register U66 which generates, CMDl-N, CMD2-N and LDlA-N and LD2A-N to the Formatter function.

5-587. Which the Mag Tape Controller is slaved to read its control register, the Mag Tape Controller address receiver and recognition circuit generates AABL-P (waveform A, figure 87) and ARED-P (waveform B, figure 87) which enables G15. The Mag Tape Controller INFIBUS access circuit then generates STRA-P (waveform C, figure 87) which activates G15 and the output of G15 enables G13, G14 and G16. The Mag Tape Controller address receiver and recognition circuit then generates AMAS-P (waveform D, figure 87) which activates G13 and G13 generates DBRA-P (waveform E, figure 87). At the same time, the Mag Tape Controller data input and selector circuit generates DOOA-N through D15A-N, representing the control word, which is routed to the data bus driver/receivers U69, U70, U79 and U80. DBRA-P strobes data bus driver/receivers U70 and U80 which couple DOOA-N through DO5A-N, D08A-N, and DO9A-P to the INFIBUS data lines.

5-588. To load data into the Mag Tape Controller data register, the Mag Tape Controller must first be reset and then the Mag Tape Controller control register must be loaded with a write control word. This causes WBAS-P and CR1S-P to be generated, as discussed previously, which enables G10. When the Mag Tape Controller is slaved to write data into its data register, DBOO-N through DBO7-N, representing the data word, are present on the INFIBUS. DBOO-N through DB07-N are inverted and routed to the output data register U57 by the data bus driver/receivers U69, U70 and U80. The Mag Tape Control' address receiver and recognition circuit then generates ADAT-P and AWRT-P. ADAT-P enables G10 and AWRT-P activates G10 which generates WDRB-N. WDRB-N triggers and loads the output data register U57 with the data word. Also, WDRB-N is routed to the Mag Tape Controller read/write control status circuit and this causes WBAS-P to be removed which disables G10. G10 removes WDRB-N and the outputs of the output data register U57 is coupled through data drivers U62, U63 and U72 (DRl shown) which generates ODOO-P through OD07-P. ODOO-P through OD07-P represents the data word which is routed to the Formatter Function.

5-589. When the Mag Tape Controller is slaved to read data out of its data register, the Mag Tape Controller address receiver and recognition circuit generates AABL-P and ARED-P. AABL-P and ARED-P enables G15 and then the Mag Tape Controller INFIBUS access circuit generates STRA-P which activates G15. The output of G15 enables G13, G14 and G16 and then the Mag Tape Controller address receiver and recognition circuit generate AMAS-P and ADAT-P. AMAS-P activates. G13 which generates DBRA-P. ADAT-P activates G14 and G16 which generates DBRB-P and DBRC-P, respectively. At the same time, the Mag Tape Controller data input and selector circuit generates DOOA-N through D15A-N which are routed to the data bus

driver/receivers U69, U70, U79, and U80. DBRA-P, DBRB-P, and DBRC-P strobes the data bus driver/receivers which cause the data to be routed to the INFIBUS data lines DBOO-N through DB15-N.

5-590. When the Block Transfer Adapter is initialized, the Mag Tape Controller is slaved by the Block Transfer Adapter to present **data** to the Formatter function or to the INFIBUS. The following two paragraphs discuss a write and a read operation when the Block Transfer Adapter in initialized.

5-59 1. For a write operation, the Mag Tape Controller is cleared and a write control word is loaded into the control register. This causes WBAS-P (waveform A, figure 88) and CRlS-P (waveform B, figure 88) to be generated which enables G10, as previously discussed. The Block Transfer Adapter performs a DDT which slaves the Core Memory Controller to read data from the Core Memory. Also, the Block Transfer Adapter generates BTA2-N (waveform C, figure 88) which is inverted by inverter I13. The output of I13, BONA-P, (waveform D, figure 88) enables G10, G13, G14, and G16. BONA-P is also routed to the Mag Tape Controller read/write control status circuit. The Core Memory Controller presents data on the INFIBUS and DBOO-N through DB07-N is inverted and routed to output data register U57 by data bus driver/receivers U69, U70 and U80. When the DDT is completed, the Mag Tape Controller INFIBUS access circuit generates BDNA-P (waveform E, figure 88) which activates G10. G10 generates WDBR-N (waveform F, figure 88) which triggers and loads output data register U57 with data. Also, WDRB-N is routed to the Mag Tape Controller read/write control status circuit which causes WBAS-P to be removed. G10 is disabled and WDRB-N is removed. The output of output data register U57 is coupled through data drivers U62 and U63. This action generates ODOO-P through OD07-P which is routed to the Formatter Function. The Formatter Function accepts **the** data **and** then the cycle is repeated until all data required is transferred.

5-592. For a read operation, CROS-P (waveform A, figure 89) is generated which enables G13, G14 and G16, as previously discussed. The Formatter function is notified of a read operation and then the Formatter function presents data to the Mag Tape Controller. This causes the Mag Tape Controller data input and selector circuit to generate DOOA-N through D15A-N which is routed to data bus driver/receivers U69, U70, U79 and U80. The Block Transfer Adapter initiates a DDT and generates BTA2-N (waveform B, figure 89) which is inverted by I13. I13 generates BONA-P (waveform C, figure 89) which enables G10, and activates G13, G14 and G16. BONA-P is also routed to the Mag Tape Controller read/write control Stat us circuit. G13, G14, and G16 generates DBRA-P, DBRB-P, and DBRC-P, respectively. This strobes data bus drivers/receivers U69, U70, U79, and U80 which couples the data onto the INFIBUS data lines. The Block Transfer Adapter then completes the DDT by slaving the Core Memory Controller to write the data into the Core Memory. The cycle is repeated until all data required is transferred.

5-593. For a write or read operation, when all data required is transferred, the Block Transfer Adapter generates BTA4-N on the INFIBUS. BTA4-N disables G8 and is routed to the Mag Tape Controller INFIBUS access circuit or CATS-P and the Mag Tape Controller initiates an interrupt.

5-594. When the Mag Tape Controller performs an interrupt, the Mag Tape Controller address (device number) is placed on to the INFIBUS data lines. The Mag Tape Controller INFIBUS access circuit generates BOLA-P and BOLA-P activates G13, G14, and G16 which generate DBRA-P, DBRB-P, and DBRC-P, respectively. At the same time, the Mag Tape Controller data input and selector circuit generates D00A-N through D15A-N, representing the Mag Tape Controller address, which is couted to the data bus driver/receivers U69, U70, U79) and! U80. DBRA-P, DBRB-P, and DBRC-P strobe data bus driver/receivers U69, U70, U79,

and U80 D15A-N which couples DOOA-N through to the INFIBUS data lines.

5-595. MAG TAPE CONTROLLER READ/ WRITE CONTROL STATUS CIRCUIT.

5-596. General. The Mag Tape Controller read/write 'control status circuit controls the transferring of data to or from the Formatter. It controls writing or reading operations of data with the Formatter and provides error indications for timing errors and overrun conditions.

5-597. Detail Analysis (see figure 90). When the master reset pulse is generated on the INFIBUS or when the MAG TAPE CONTROLLER status register is written, the Mag Tape Controller data output and control register circuit generates GRSA-N and GRSC-P. GRSA-N resets flip-flop FF4, and activates gate G7 which resets flip-flop FF3. GRSC-P activates gate G2 which presets flip-flop FF1. FF1 then generates WBAS-P and WBAR-N. WBAS-P enables half of gate G12 and is also routed to the Mag Tape Controller data output and control register circuit. WBAR-N disables gate G4 and is also routed to the Mag Tape Controller address receiver and recognition circuit.

5-598. With operation control word stored in the Mag Tape Controller data output and control register circuit, CRIS-P is generated which enables G4 and activates G12. G12 generates PDSA-N which is routed to the Mag Tape Controller data input and selector circuit and Mag Tape Controller INFIBUS access circuit. PDSA-N is also coupled through driver DR1 which generates BTAl-N.

5-599. When the Formatter is ready to accept the data word, it generates WDDC-N which activates gate G1. G1 enables G4. The output of gate G13 is always low which keeps half of gate G14 disabled. Also, inverter I5 inverts the output of G13 and enables G4.

5-600. To present a data word to the Formatter, the Block Transfer Adapter slaves the Mag Tape Controller which causes the Mag Tape Controller data output and control register circuit to generate **WDRB-N,** WDRB-N triggers and clears FFl which removes WBAS-P and WBAR-N, and G12 is disabled and G4 is activated. Gate G4 activates G5 which activates I1 which generates WDGA-N to the Formatter. The Formatter accepts the data word and removes WDDC-N which disables Gl. G4 is disabled and WDGA-N is removed. Also, the high to low transition output of Gl sets single-shot SSl which activates G2.

5-601. G2 presets FFl which generates WBAS-P and WBAR-N and the cycle previously discussed is repeated for the next data word.

5-602. Read. With a read operation control word stored in the data output and control registed circuit, WRCO-P, CROA-P, and CROS-P are generated. WRCO-P and CROA-P activates gate G3 which presets FF2. CROS-P enables gate G11, half of gate G12, half of gate G14, and the set input of FF2. The 1 output of FF2 is inverted by inverter I2 which disables G11.

5-603. The Formatter presents a data word to the Mag Tape Controller which causes the Mag Tape Controller data input and selector circuit to generate RDSP-P and RDST-N when IDSB-N is generated. RDSP-P triggers FF4 and activates gate G10 which resets FF2. RDST-N is inverted by inverter I4 which enables G11. With FF2 reset, 12 activates G11 and G11 generates ISB-N which is routed to the Formatter to indicate a successful transfer.

5-604. The Mag Tape Controller data input and selector circult removes RDSP-P, which disables G10, and RDST-N, which triggers sets FF3. The 1 output of FF3 enables the set input of FF4 and also activates G12, which generates BTAl-N. With RDST-K removed, I4 disables G11 which removes ISB-N.

5-605. The Block Transfer Adapter slaves the Mag Tape Controller to place the data

word onto the INFIBUS. This **causes the** Mag Tape Controller data output and con**trol** register circuit to generate BONA-P which enables gate G6. When the transfer **of the data word by the** Block Transfer Adapter is completed, the **Mag Tape** Controller address receiver and recognition circuit generates BDNA-P.

5-606. BDNA-P activates G6 and the output of G6 activates G7 which resets FF3. This causes G12 to be disabled which removes BTAl-N. Afterwards, BDNA-P is removed by the Mag Tape Controller INFIBUS access circuit which disables G6. This causes G7 to be disabled and the low-to-high transition output of G7 triggers and sets FF2. The cycle for reading the next word from the Formatter is repeated as discussed.

5-607. If during the read operation cycle the Formatter is not ready to transfer data, it generates RDNR-P which disables gate G8. G8 generates RDNR-N which activates gate G9 and G9 activates G10 and G14. G10 resets FF2 and G14 generates EROR-N. The read operation cycle is inhibited and the Mag Tape Controller INFIBUS access circuit initiates an interrupt to indicate a read timing error.

5-608. If the Block Transfer Adapter does not slave the Mag Tape Controller to present the data word on to the INFIBUS before the next data word is presented by the Formatter, an overrun condition occurs. The previous data word is destroyed. FF3 is not reset by G7, as discussed, and RDSP-P triggers and sets FF4 which generates RTER-N. RTER-N activates G9 which activates GlO and G14. G10 resets FF2 and G14 generates EROR-N. The read operation cycle is inhibited and the Mag Tape Controller INFIBUS access circuit initiates an interrupt to indicate an overrun condition,

5-609. I/O CONTROLLER CLOCK CIRCUIT.

5-610. General. The I/O Controller clock circuit divides the INFIBUS clock signal, CLKA-N, by three and supplies timing pulses to the I/O Controller interface circuit and the **I/O** Controller INFIBUS access logic circuit.

5-611. Detail Analysis (see figure 91). The INFIBUS clock signal, CLKA-N (waveform A, figure 92), is inverted by inverter I3 and applied to the trigger inputs of flip-flops FFl and FF2. For this discussion assume FFl and FF2 are initially in the reset state. With FF1 and FF2 reset, gates Gl and G2 are disabled. The output of G2 prevents FF2 from being set. The first positive going edge out of I3 sets FF1. The 0 output of FF1 (waveform B, figure 92) activates G2 and the 1 output of FFl enables Gl. The second positive edge out of I3 clears FFl and sets FF2. The 0 output of FF2 now activates G2 and the 1 output of FF2 enables Gl. The third positive going edge out of I3 sets FFl (FF2 remains set because G2 activated). With FF1 and FF2 set, G1 is activated. After the inherent gate delay of Gl, the output of Gl goes low which resets FF1 and FF2. Resetting FFl and FF2 causes the entire sequence to repeat itself. The 1 output of FF2, Q2-P (waveform C, figure 92), is inverted by inverters I2. and I1 which generate Ql-N and Q3-N, respectively.

5-612. I/O CONTROLLER ADDRESS RECOGNITION, DONE, AND RESET CIRCUIT.

5-613. General. The I/O Controller address recognition, done, and reset circuit detects when the I/O Controller is being addressed (slaved) using address bits AB04-N through AB15-N and decodes address bits ABOO-N through AB03-N to select either the Rapid Memory Reload (RMR), Register Sender Junctor (RSJ), or Call Combiner Logic (CCL) functions. The i/O Controller address recognition, done, and reset circuit strobes the data command word through the I/O Controller data circuits. The I/O Controller address recognition, done, and reset circuit also generates the DONE-N signal that is routed to INFIBUS and generates reset signals that are routed to the RMR, RSJ, and CCL functions and to the I/O Controller INFIBUS access logic circuits and data circuits.

5-614. Detail Analysis (see figure 93). When the master reset pulse, MRES-N, is

detected on the INFIBUS, the I/O Controller INFIBUS access circuit generates GEN RESET-N. GEN RESET-N activates gates G9, G12, and Gl5. The output of G9 is inverted by inverter I5 which generates RSJ RESET-N and RSJ RESET. Activating G12 generates CCL RESET-N and CCL RESET and activating G15 generates RMR RESET-N and RMR RESET.

5-615. When address F88X l6 (AB07-N and AB11-N through AB15-N low) is on the INFIBUS address lines gate G4 is activated. Address bits AB12-N through AB15-N are coupled through and inverted by the address receivers U13, U26, U39, and US2 to activate gate G4. Address bits AB08-N through AB11 -N are inverted and coupled through the address receivers and address bits AB08-N through AB10-N are also inverted by inverters I2, I3, and I4 to activate gate G7. Address bits AB04-N through ABO7-N are inverted and coupled through the address receivers and address bits AB04-N through ABO6-N are also coupled through inverters I9 through Ill to activate gate G10. The outputs of G4 and G7 activate gate G5 and the output of G10 is inverted by inverter I8. The high outputs of G5 and I8 activate gate G6 which enables gates G13, G18, G17, G16, and G19 and generates F88-N. F88-N causes the I/O Controller INFIBUS access circuit to generate BUSEN-P which enables gate G23.

5-616. Address bits ABOO-N through AB03-N are inverted and coupled through the address receivers and routed to BDC-to-decimal decoders U21 and U22. The AB03-N output of the address receivers is inverted by inverter I16 before it is applied to BCD-to-decimal decoder U22. If ABOO-N through AB03-N are low (decimal 0), the 0 output of the BCD-to-decimal decoder U21 activates G18. If AB02-N is low and ABOO-N, ABOl-N, and AB03-N are high (decimal 2), the 2 output of BCD-to-decimal decoder U21 activates G17. If A802-N is low and ABOO-N, ABOl-N and AB03-N are high (decimal 4), the 4 output. of BCD-to-decimal decoder U21 activates G16. If ABOl-N and AB02-N are low and ABOO-N and AB03-N are high (decimal 6), the 6 output of BCD-to-decimal decoder U21 activates G13. If AB02-N and AB03-N are low and ABOO-N and ABOl-N are high (decimal 12), the 12 output of BCD-to-decimal decoder U22 activates G19.

5-617. When STRB-P from the INFIBUS access logic circuits goes high, register U58, flip-flop FFl and gate G22 are enabled and single shot SSl is triggered. 175 nsec after SS1 is triggered its output returns to high which triggers register U58 clocking the output of G13, G18, G17 and G19, or G16 into the register U58.

5-618. When the I/O Controller is being written into, under control of the stored software program, to select the RMR, CCL, or RSJ function; RITE-P is high which enables gates Gl through G3 and G8, G11, and G14.

5-619. When the I/O Controller is being written into, under software program control. to select the RSJ function, G18 is activated (ABOO-N through AB03-N equal decimal 0). When register U58 is triggered by SSl, the Q2 output of register U58 goes high which activates G8. The output of G8 activates G9 which generates RSJ RESET-N and RSJ RESET, as explained previously. The Q2 output of register U58 is also inverted by inverter I6 which generates RSJ STAT SEL-N and the output of I6 is inverted by inverter I7 which generates RSJ STAT SEL. Under these conditions the RSJ function is selected and reset. RSJ STAT SEL-N activates gate G20 which triggers single shot SS2. 600 nsec after SS2 is triggered, FF1 is set. Setting FF1 activates G21 which activates G22. The output of G21 is also inverted by inverter I17. The output of I17 is delayed 50 nsec by delay DL1 which causes G22 to be disabled 50 nsec after it is activated. The 50 nsec positive pulse out of G22 is inverted by inverter I18. The output pulse of I18 activates gate G23 which generates DONE-N notifying the CPU that the operation is complete. The output of G23 is also inverted by inverter I19, causing DONE-P to go high which is routed to the I/O Controller INFIBUS access logic circuit. Generating DONE-N causes the CPU to remove STRB-N. STRB-P goes low which resets register U58 and FF1, and disables G22.

5-620. When the I/O Controller is being written into, under control of the stored software program, to select the CCL function, G17 is activated (ABOO-N through AB03-N equals decimal 2). When register U58 is triggered by SSl, the Q3 output of register U58 goes high which activates G11. The output of G11 activates G12 which generates CCL RESET-N and CCL RESET, as explained previously. The Q3 output of register U58 is also inverted by inverter I12 which generates CCL STAT SEL-N and the output of I6 is inverted by inverter I7 which generates CCL STAT SEL. Under these conditions the CCL function is selected and reset. CCL STAT SEL-N activates G20 which causes DONE-N to be generated and register U58 and FFl to be reset, as explained previously.

5-621. When the I/O Controller is being written into, under control of the stored software program, to select the RMR function, G16 is activated (ABOO-N through AB03-N equals decimal 4). When register U58 is triggered by SSl, the Q4 output of register U58 goes high which activates G14. The output of G14 activates G15 which generates RMR RESET-N and RMR RESET, as explained previously. The Q3 output of register U58 is also inverted by inverter I14 which generates RMR STAT SEL-N and the output of I14 is inverted by inverter I15 which generates RMR STAT SEL. Under these conditions the RMR function is selected and reset. RMR STAT SEL-N also activates G20 which causes DONE-N to be generated and register U58 and FF1 to be reset, as explained previously.

5-622. When the data command word on the INFIBUS data lines is to be strobed (written) into the I/O Controller data circuits, RITE-P is high which enables G1, G2, G3 and G26. Gate G13 is activated (AB00-N through AB03-N equals decimal 6). When register U58 is triggered by SS1, the Q1 output of register U58 activates G1, G2, and G3. The outputs of G1 (RSJ CMND CLK-P), G2 (CCL CMND CLK-P), and G3 (RMR CMND CLK-P) strobe the data command word into the I/O Controller data circuits. The Q1 output of register U58 is also inverted by inverter I1 generating CMND SEL-N which activates G21 causing DONE-N to be generated and register U58 and FFl to be reset as explained previously.

5-623. If RITE-P is high and decimal 12 is on the INFIBUS address lines ABOO-N through AB03-N, **G19** is activated and the output of register U58, RMR PDT SEL-P, goes high. RITE-P enables gate **G26** and HMR PDT SEL-P activates **G26** which triggers single shot SS3. 175 nsec after SS3 is triggered, FF2 sets which activates gate G27 and enables gate G24. The output of G27, RMR DT REQ, notifies the RMR function that an RMR data request is being made. In response ***to*** RMR DT REQ going low, the RMR function causes RMR DT RES to go low. RMR DT RES is inverted by inverter I20 which activates G24. The output of G24 activates G21 which causes DONE-N to be generated as explained previously.

5-624. If READ-P is high and decimal 12 is on the INFIBUS address lines ABOO-N through ABO3-N, RMR PDT SEL-P is generated as explained previously. READ-P enables gate **G26** and RMR PDT SEL-P activates gate G26. The output of G26 enables gate G25 and activates G27. The output of G27, RMR DT REQ, causes the RMR function to generate RMR DT RES. RMR DT RES is inverted by I20 which activates G25. The output of G25 causes DONE-N to be qenerated 600 nsec after G25 is activaated, as explained previously.

5-625. I/O CONTROLLER DATA CIRCUIT.

5-626. General. The I/O Controller data circuit receives the data signals (under software program control) from the INFIBUS and decodes these signals to generate the commands to the RSJ, CCL, and RMR functions when the I/O Controller is being written into.

5-627. Detail Analysis (see figure 94). RSJ RESET-N from the I/O Controller address recognition, done, and reset circuit activates gate G5 which resets flip-flops FF2 and FF4. CCL RESET-N activates gate G11 which resets flip-flop FF8. The output of G11 activates gate G12 which resets

flip-flops FFl, FF3, FF5 through FF7 and FF9. RMR RESET-N activates gate G18 which resets flip-flops FF10 through FF13 and FF14.

5-628. When the I/@ Controller is being written into (RITE-N low) and when address recognition occurs, RSJ CMND CLK-P, CCL CMND CLK-P, and RMR CMND CLK-P are generated simultaneously by the I/O Controller address recognition, done and reset circuit. The leading edges of RSJ CMND CLK-P, CCL C MND CLK-P, and RMR CMND CLK-P trigger FFl through FF14, clocking the associated input data into the flip-flops. On the trailing edges of RSJ CMND CLK-P, CCL CMND CLK-P, and RMR CMND CLK-P (when I/O Controller address removed from INFIBUS address lines) the output of the appropriate flip-flops change state generating the appropriate command word to the RSJ, CCL, or RMR functions.

5-629. If data bit DBOO-N is low and data bit DBOP-N is high, DBOO-P is high and DBOl-P is low. DBOO-P enables gates G1 and G2 and enables FF2 to be set by RSJ CMND CLK-P. DBOl-P disables G1 and is inverted by inverter I7. The output of I7 activates G2 which enables FF4 to be cleared by RSJ CMND CLK-P, if necessary. The trailing edge of RSJ CMND CLK-P sets FF2 and ensures FF4 is cleared. The output of FF2 is inverted by inverter I3 causing DORSJ to go low. DORSJ notifies the RSJ function to perform a traffic or call data collection operation. When DBOO-N and DBOl-N are low, DBOO-P and DBOl-P are high which activates gate G1. Under these conditions, the trailing edge of RSJ C MND CLK-P sets FF2 and FF4. With FF2 and FF4 set, DORSJ and RSJ INT INH are generated by inverters I3 and I5, respectively. With DORSJ and RSJ INT INH low, the RST function is enabled by DORSJ and INT INH prevents the RSJ function from generating a request for INFIBUS access.

5-630. Data bits DB02-N through DB07-N are coupled through and inverted by data bus receivers U64 and U78, generating DB02-P through DB07-P. If any one or more of the data bits DBOO-P through DB06-P are high the associated flip-flop, FFl, 3, 5, 6, 7, 8 is set by CCL CMND CLK-P. Also, if any one or more, but not ail data bits DB02-P through DBOG-P are low, the output of gate G6 is low which disables gate G9. This low output of G6 is inverted by inverter I11 which enables gates G7 and G8. If DB07-P is high at this time, G7 is activated enabling FF8 to be set. If DBO7-P is low at this time, it is inverted by inverter I13 which activates G8 enabling FF8 to be cleared, if necessary, by CCL CMND CLK-P. If data bits DB02-P through DBOG-P are low, the output of G6 is high, which enables G9. If DB07-P is high at this time, G9 is activated. The output of G9 enables G10 to be activated by CCL CMND CLK-P. The output of G10 activates G11 which resets FF8. The output of G11 also activates G12 which resets FFl, FF3, FF5 through FF7 and FF9. If DB15-N is low, DB15-P is high which enables FF9 to be set by CCL CMND CLK-P. The outputs of FFl, FF3, and FF5 through FF8 are inverted by inverters I1 through I12, respectively. The output of I1, DOTST, is routed to the CCL function. The output of I4, D040, commands the CCL function to examine and update all transition leads. The output of I6, D01 commands the CCL function to examine and update all transition and 1 second usage/duration leads. The output of I9, D010, commands the CCL function to examine and update all transition, 1 second and lu second usage/duration leads. The output of I10, DOCALL, commands the CCL function to operate in the call data collection mode. The output of I12, CCL INT INH, prevents the CCL function from requesting INFIBUS access,, The output of FF9 is inverted by inverter I15. The output of I15, TOG, specifies the exact location in Core Memory where the last transition count is stored. When SCAN COMPLETE (high) is received, it is inverted by inverter I14 which activates G12. The output of G12 resets FFl, FF3, FF5 through FF7 and FF9.

5-631. When DB08-P is high, FF10 is enabled to be set by RMR CMND CLK-P. Data bits DB08-N throuqh DB13-N and DB15-N are coupled through and inverted by the data bus receivers U91 and U65. DB09-P enables FF11, DB10-P enables FF12,

and DB15-P enables FF13 to be set when RMR CMND CLK-P is generated. If DB11 P and DB12-P art- both low, FF13 is cleared, if necessary, when RMR CMND CLK-P is generated. If DB11-P is high and DB12-P is low, FF13 toggles when RMR CMND CLK-P is generated. If DB11l-P is low and DB12-P is high, FF13 does not change state when RMR CMND CLK-P is generated. If DB11-P and DB12-P are high, FF13 is set by RMR CMND CLK-P. If any one or rnore, but not all, data bits DB08-P through DB10-P are low, the output of G13 is low which disables gate G16. The low output of G13 is inverted by inverter I22 which enables gates G14 and G15. If DB13-P is high at this time, G 14 is activated which enables TF14 to be set by RMR CMND CLK-P. If DB13-P is low, it is invertcd by inverter I24 which activates G15. The output of G15 enables FF14 to be cleared, if necessary, by PMR CMND CLK-I'. If data bits DBO8-P through DB10-I' are low the output of G13 is high which **enables gate** G16. If DB13-P is high at this time G16 is activated. The output of G17 activates G18 which rcsets FF10 through FF14. The outputs of FF10 through FF13 and FF14 are inverted by **inverters** I17 through I20 and I23, respectively. The output of I17, $\overline{\text{DONOR}}$, commands the RMR function to operate in the new data read mode. The output of I18, $\overline{\text{DORDR}}$, commands the RMR function to operate in the revise data read mode. The output of I19, DOMDW, commands the RMR function to operate in the writc **mode.** The output of 120, DOSED, notifies the RMR function that A timing error or detected error has occurred. **The** output of I23, $\overline{\text{RMR INT INH}}$, prevents the RMR function from requesting INFIBUS access.

5-632. I/0 CONTROLLER INTERFACE CIRCUIT.

5-633. General. **The I/O Controller interface** circuit detects when the RSJ, CCL, or RMR functions are requesting INFIBUS access and **notify the RSJ, CCL or RMR functions when they can gain INFIBUS access.** I/O Controller interface circuit grants access to RSJ, RMR, and CCL by controlling which circuit has access to the common Data Highway.

5-634. Detail Analysis (see figure 95). If no request is being generated for INFIBUS access, RSJ BUS REQ, CCL BUS REQ, and RMR BUS REQ are low and the shift register U54 is free-running. Clock pulses, Q1-N (waveform A, figure 96), are inverted by inverter I4 and the output of I4 (waveform B, figure 96) is inverted by inverter I5. Because RSJ BUS REQ, CCL BUS REQ, and RMR BUS REQ are low, the outputs of register U66 disable gates G5, G6, and G7. The output of I4 is constantly triggering shift register U54. For initial condition, assume OAA-P (waveform C, figure 96), OBB-P (waveform D, figure 96), OCC-P (waveform E, figure 96), and ODD-P (waveform F, figure 96) are low which disables gates G3 and G4. The high output of G4 enables the parallel load (L) input and parallel (A) input of shift register U54. The high output of G4 also activates G2 which disables the shift (S) input of shift register U54 which prevents data from shifting serially through shift register U54. Under these conditions, the first negative going edge out of I4 causes OAA-P to go high which activates G3. The output of G3 activates G4 which disables the L and A inputs of shift register U54 preventing any more parallel data from being loaded into shift register U54. The output of G4 also disables G2 which enables the data (OAA-P) now stored in shift register U54 to be shifted serially. The next negative going edge out of I4 causes OAA-P to return to low and OBB-P to go high. OBB-P activates G3 causing shift register U54 to operate in the serial shift mode as explained previously. The third negative going edge out of I4 causes OBB-P to go low and OCC-P to go high. OCC-P activates G3 causing the shift register to continue to operate in the serial shift mode. The fourth negative going edge out of I5 causes OCC-P to go low and ODD-P to go high. ODD-P activates G4, shift register U54 continues to operate in the serial shift mode and with ODD-P high the SA input of shift register U54 is high. The fifth negative going edge out of I4 causes OAA-P to go high and ODD-P to go low. The sequence of operation repeats itself as long as the RSJ BUS REQ, CCL BUS REQ, and RMR BUS REQ signals remain low.

5-635. When CCL BUS REQ (waveform G, figure 96) goes high, the next positive going edge out of IS triggers this level into register U66 which enables gate G6. When OBB-P goes high, G6 is activated which activates Gl. The output of Gl activates G2 causing shift register U54 to stop shifting data serially. OBB-P is activating G3 which disables the parallel load input of shift register US4 as explained previously The output of G6 is inverted by inverter Ii which causes CCL BUS ACK to go high. The output of G6 is also inverted by inverter I2 which activates the CCL enable line driver U79 causing CCL EN to go high and CC EN to go low. The I/O Controller interface circuits remain in this state until CCL BUS REQ returns to low. The next positive going edge out of I5 now triggers this level into register U66 which disables G6. The output of G6 now disables Gl which disables G2. The output of G2 now allows shift register U54 to resume its normal sequence of operations.

5-636. Operation of the I/O Controller interface circuit when RMR BUS REQ goes high is similar to when CCL BUS REQ went high, except gate G7 is activated and shift register U54 operations cease when OCC-P is high. The output of G7 is also inverted by inverters I8 and I3, causing RMR BUS ACK and RMR to go high for as long as RMR BUS REQ is high.

5-637. Operation of the I/O Controller interface circuit when RSJ BUS REQ goes high is similar to when CCL BUS REQ went high, except gate G5 is activated and shift register operations cease when OAA-P is high. The output of G5 is inverted by inverter I6 which causes RSJ BUS ACK to go high. The output of G5 is also inverted by inverter I1 which enables RSJ enable 1, RSJ enable 2, and RSJ enable 3 line drivers U79 and U40. RSJ BUS ACK is high and the RSJ enable 1, RSJ enable 2, and RSJ enable 3 are enabled for as long as RSJ BUS REQ is high as explained previously when CCL BUS REO was high. When RSJ SEL 1 goes high, RSJ enable 1 line driver U79 is activated which causes RSJ EN1 to go high and $\overline{\text{RSJ EN 1}}$ to go low for as long as RSJ SEL 1 and RSJ BUS REO are both high. When RSJ SEL 2 goes high, RSJ enable 2 line driver (40) is activated which causes RSJ EN 2 to go high and RSJ EN 2 to go low for **as long** as RSJ SEL 2 and RSJ BUS REQ are both high. When RSJ SEL 3 goes high, RSJ enable 3 line driver 40 is activated which causes RSJ EN 3 to go high and $\overline{\text{RSJ EN 3}}$ to go low for as long as RSJ EN 3 and RSJ BUS REQ are both high.

5-638. I/O CONTROLLER INFIBUS ACCESS LOGIC CIRCUIT.

5-639. General. The I/O Controller INFIBUS access logic circuit detects when the RSJ or CCL function is requesting a direct memory access (DMA) request and, in response, generates a direct data transfer (DDT) INFIBUS access request. Also, during a DMA request, the INFIBUS access logic circuit detects whether the RSJ or CCL function is requesting a read (reading data from INFIBUS) or write (writing data onto INFIBUS) operation. The I/O Controller infibus access logic circuit also detects when the RSJ, CCL, or RMR function is generating an interrupt request and, in response, generates a level 2 interrupt INFIBUS access request. The INFIBUS access logic circuits also couple the error signal (QUIT-N) to the RSJ and CCL functions.

5-640. Detail Analysis (see figure 97). The master reset pulse, MRES-N, is inverted by inverters I9 and I10. The output of I10, GEN RESET-N (waveform B, figure 98) is routed to the I/O Controller address recognition, done, and reset circuit and resets register U15 which disables gates G3, G5, G7, G9, and G11. GEN RESET-N is also inverted by inverter I5 which activates gate G14 and enables the parallel load (L) input of shift register U4. The output of G14 disables the serial shift input (S) of shift register U4. Disabling G3, G5, G7, G9 and G11 disables gates G4, G6, G8, G10, and G12. The low output of gate G15, DMAREQ-P, is inverted by inverter Ill. The output of Ill is inverted by I13 which resets flip-flop FF3. The low output of Gl6, INTREQ-P, is inverted by inverter I16. The output of I16 is inverted by inverter I18 which resets flip-flop FF6. The low output of Gl3 activates gate G2

which resets flip-flop **FF2.** Resetting FF2 **disables gates G4, G6, G8,** G10, and G12 **and STRB ENBL-N** (high) activates G33 **which** resets flip-flops FF9, **FF11,** and **FF12.** The **low** output of G13 is also inverted by inverter I3 which causes SERV REQ-N to go high. SERV REQ-N is inverted by inverter **I22** which resets flip-flop FF8, and by inverter I21 which resets flip-flops **FF4; FF5,** and FF7. Resetting FF8 causes SELECT-P to go low which resets FFl. With FF4 and FF5 reset, gate G21 is enabled to couple the precedance pulse, PCDA-P, from the INFIBUS to the INFIBUS as PCDB-P.

5-641. With the L input of shift register U4 enabled and the S input disabled, the first trailing edge of Q2-P (waveform A, figure 90) triggers shift register U4 which parallel loads shift register U4. Parallel loading of shift register U4 causes OA-N (waveform C, figure 98) OB-N (waveform D, figure 98), OC-N (waveform E, figure 98), and OD-N (waveform F, figure 98) to go high which activates gate G17 causing OE-N (waveform G, figure 98) to go low. When GEN RESET-N returns to high, which is inverted by I5, G14 is disabled and the L input of shift register U4 is also disabled. If RSJ DMA REQ, CCL DMA REQ, RSJ INT REQ, CCL INT REQ, and RMR INT REQ are all low, the outputs of register U15 all remain low holding G3, G5, G7, G9, and G11 disabled which holds G13 disabled. The low outputs of G13 and I5 disable G14. The high output of G14 enables the S input of shift register U4. The serial input (SA) of shift register U4 at this time is low. Under these conditions, the first trailing edge of Q2-P, after GEN RESET-N goes high, causes OA-N to go low which disables G17. This causes OE-N to go high. The next trailing edge of Q2-P causes OA-N to go high and OB-N to go low. The next trailing edge of Q2-P causes OB-N to go high and OC-N to go low. The next trailing edge of Q2-P causes OC-N to go high and OD-N to go low. The next trailing edge of Q2-P cause; OD-N to go high which activates G17 again. OA-N through OE-N are inverted by inverters I2 and I4 through I8 which sequentially causes G3, G5, G7, G9, and Gil to be enabled. The process repeats itself until **an RSJ DMA REQ,** CCL DMA REQ, RSJ INT **REQ,** CCL INT **REQ,** or RMR INT REQ input is detected.

5-642. When the RSJ function is requesting **a** direct memory access, RSJ DMA REQ (waveform H, figure 99) goes high. The trailing edge of Q2-N clocks the high level of RSJ DMA REQ into register U15 which enables G3. G3 is activated when OA-N goes **low.** The output of G3, Rl-N, enables G4 and activates G13 and G15. The output of G13 activates G14 which disables the S input of shift register U4. Disabling the S input of shift register U4 prevents the shift register from serial shifting the data which causes OA-N to remain low for as long as Gl is activated. The high output of G13 disables G2 which allows FF2 to be set when triggered. The high output of G13 is also inverted by I3 causing SERV REQ-N to go low. SERV REQ-N is inverted by I22 which enables FF8 to be set. SERV REQ-N is also inverted by I21 which enables FF4, FF5, and FF7 to be set and activates gate G31. The output of G31, BUSEN-P, enables bus driver/receivers U38 (G30 shown) and bus drivers U51 (G25 shown). The output of G15, DMA REQ (waveform I, figure 98), is inverted by I11. The output of I11 is inverted by I13 which enables FF3 to be set. If no other function is requesting a direct data transfer INFIBUS request, SELD-N is high which is inverted by inverter I14. The output of I14 disables gate G19 and is inverted by inverter I15. The output of I15 enables gate G18. The output of Ill is also delayed 50 nsec by DLl and then inverted by inverter I12. The output of I12 activates G18 which sets FF3. The 1 output of FF3 enables G19 and the 0 output of FF3 is coupled through bus drivers U51 which generates SRLD-N. In response to SRLD-N the Bus Controller causes SELD-N to go low which is inverted by I14 and I15. The output of I15 disables G18 and the output of I14 activates G19 which sets FF4 and enables gates G20 and G26. The 0 output of FF4 disables G21 preventing the precedance pulse, PCDA-P, (when received) from being coupled through G21. When PCDA-P is received, G26 **is** activated which sets FF7 and FF8 and activates G20. The output of G20 resets FF3 which disables

G19. The output of G19 disables G20 after FF3 has reset. The 0 output of FF7 is coupled through bus drivers U51 to the INFIBUS as SACK-N. The 0 output of FF8 disables gates G18 and G22. The 1 output of FF8, SELECT-P, enables gate G28, sets FF2, and triggers single shot SS2. Setting FF2 enables gate Gl and generates STRB ENBL-N. STRB ENBL-N disables G33 which allows flip-flops FF9, FF11, and FF12 to be set when triggered. SS2 resets 125 nsec after it was triggered which triggers and sets FFll. The output of FFll activates gate G29 (STRB-N high) which triggers SSl and sets FF12. The 0 output of FF12, RDY NXT CYCLE-N, activates Gl which activates G4. G4 generates RSJ DMA ACK which notifies the RSJ function that the direct data transfer request has been acknowledged. If the RSJ function is requesting a write operation, RSJ WRITE is high which enables gate G34. Rl-N is inverted by inverter I26 which activates G34. The output of G34 enables G32. The 1 output of FF12, RDY NXT CYCLE-P, enables FFl to be set and activates G32. The output of G32 is coupled through bus driver/receivers U38 generating RITE-N and enabling FF10 to be set. 125 nsec after SSl is triggered, the output of SSl sets FF9. The 0 output of FF9 is coupled through bus driver/receivers U38 which generates STRB-N and STRB-P. STRB-P is inverted by inverter I25 which disables G29. STRB-P is high which enables gate G27. The 1 output of FF9, STRB INT-P, activates G27 which resets FF4, FF5, and FF7. Resetting FF7 causes SACK-N to return to a high level and resetting FF4 and FF5 enables G21 to couple PCDA-P to the INFIBUS as PCDB-P. When the DDT is complete, the function addressed by the RSJ function generates DONE-N which causes the I/O Controller address recognition, done and reset circuit to generate DONE-P. DONE-P is inverted by inverter Il. The trailing edge of the output of I1 (trailing edge of DONE-P) sets FF1 which activates G2. **The output** of G2 resets FF2 which disables Gl. Disabling Gl causes RSJ DMA ACK to go to low which causes RSJ DMA REQ to go low. The positive going edge of Q2-N after RSJ DMA REQ) returns to **low** causes the Ql output of register U15 to return to a low level which disables G3. The output of G3, Rl-N, now goes high disabling G13 which enables the shift register U4 to serially shift data on the second negative going edge of Q2-P (due to internal delays of register U15, G2, G13, and G14), as explained previously. Rl-N also disables G15 causing DMA REQ-P to go low which holds FF3 reset. The low output of G13 is also inverted by I3 which causes SERV REQ-N to go high. When SERV REQ-N goes high FF4, FF5, FF7, FF8, and FF10 are reset and the bus driver receiver are disabled. Resetting FF2 causes STRB ENBL-N to go high which activates G33. The output of G33 resets FF9, FF11, and FF12. If the CCL function is not requesting a direct memory access and if the RSJ, CCL, and RMR functions are not requesting a level 2 interrupt INFIBUS access, shift register U4 continues to serially shift data as explained previously.

5-643. When the CCL function is requesting a direct memory access, operation is similar to when the RSJ function is requesting a direct memory access except CCL DMA REQ is high. This causes the same operations as when RSJ DMA REQ was high, except G5 is enabled by the output of register U15 and activated when OB-N is low. Activating G5 causes the shift register to stop serially shifting data when OB-N is low. When FF2 is set, G6 is activated which causes CCL DMA ACK to go high. Also, the output of G5 (R2-N) activates G15 which causes a request for a direct data transfer to be generated, as explained previously. If the CCL function is requesting a write operation, CCL WRITE is high which enables G34. When R2-N goes low and is inverted by inverter I27, G34 is activated which causes RITE-N to be generated, as explained previously.

5-644. When the RSJ function is requesting a level 2 interrupt INFIBUS access, RSJ INT REQ (waveform J, figure 98) goes high. The trailing edge of Q2-N clocks the high level of RSJ INT REQ into shift register U15 which enables G7. G7 is activated when OC-N goes low. The output of G7, R3-N, enables G8 and activates G13 and G16. The output of G13 activates G14 which dis-

ables the S input of shift register U4. Disabling the S input of shift register U4 prevents the shift register U4 from serial shifting the data which causes OC-N to remain low for as long as G7 is activated. The high output of G13 disables G2 which allows FF2 to be set when triggered, The high output of G13 is also inverted by I3 causing SERV REQ-N to go low. SERV REQ-N is inverted by I22 which enables FF8 to be set, is inverted by I21 which enables FF4, FF5, and FF7 to be set, and activates G31. The output of G31, BUSEN-P, enables bus driver/receivers U38 and bus drivers U51. The output of G16, INT REQ (waveform K, figure 98), is inverted by I16. The output of I16 is inverted by I18 which enables FF6 to be set. If no other function is requesting a level 2 interrupt INFIBUS request, SEL2-N is high which is inverted by inverter I19. The output of I19 disables gate G23 and is inverted by inverter I20. The output of I20 enables gate G22. The output of I16 is also delayed 50 nsec by DL2 and then inverted by inverter I17. The output of I17 activates G22 which sets FF6. The 1 output of FF6 enables G23 and the 0 output of FF6 is coupled through bus drivers U51 which generates SRL2-N. In response to SRL2-N the Bus Controller causes SEL2-N to go low which is inverted by I19 and I20. The output of I20 disables G22 and the output of I19 activates G23 which sets FF5 and enables gates G24 and G26. The 0 output of FF5 disables G21 preventing the precedance pulse, PCDA-P, (when received) from being coupled through G21. When PCDA-P is received, G26 is activated which sets FF7 and FF8 and activates G24. The output of G24 resets FF6 which disables G23. The output of G23 disables G24 after FF6 has reset. The 0 output of FF7 is coupled through bus drivers U51 to the INFIBUS as SACK-N. The 0 output of FF8 disables G18 and gate G22. The 1 output of FF8, SELECT-P, enables gate G28, sets FF2, and triggers single shot SS2. Setting FF2 enables G1 and generates STRB ENBL-N. STRB ENBL-N disables G33 which allows flip-flops FF9, FF11, and FF12 to be set when triggered. SS2 resets 125 nsec after it was triggered which triggers and sets FF11. The output of FF11 activates G29 (STRB-N high) which triggers SS1 and sets FF12. The 0 output of FF12, RDY NXT CYCLE-N, activates Gl which activates G8. G8 generates RSJ INT ACK which notifies the RSJ function that the level 2 interrupt request has been acknowledged. The 1 output of FF12, RDY NXT CYCLE-P, enables FFl to be set. 125 nsec after SS1 is triggered, the output of SS1 sets FF9. The 0 output of FF9 is coupled through bus driver/receivers U38 which generates STRB-N and STRB-P. STRB-P is inverted by I25 which disables G29. STRB-P is high which enables gate G27. The 1 output of FF9, STRB INT-P, activates G27 which resets FF4, FF5, and FF7. Resetting FF7 causes SACK-N to return to a high level and resetting FF4 and FF5 enables G21 to couple PCDA-P to the INFIBUS as PCDB-P. When the level 2 interrupt is complete, the CPU generates DONE-N which causes the I/O Controller address recognition, done, and reset circuit to generate DONE-P. DONE-P is inverted by inverter I1. The trailing edge of the output I1 (trailing edge of DONE-P) sets FFl which activates G2. The output of G2 resets FF2 which disables Gl. Disabling Gl causes RSJ INT ACK to go low which causes RSJ INT REQ to go low. The positive going edge of Q2-N after RSJ INT REQ returns to low causes the Q3 output of register U15 to return to a low level which disables G7. The output of G7, R3-N, now goes high disabling G13 which enables shift register U4 to serially shift data, on the second negative going edge of Q2-'P (due to internal delays of register U15, G2, G13, and G14), as explained previously. R3-N also disables G16 which causes INT REQ-P to go low which holds FF6 reset. The low output of G13 is a also inverted by I3 *which causes SERV REQ-N to go high.* When SERV REQ-N goes high FF4 FF5, FF7, FF8, *and FF10* are reset. Resetting FF2 causes STRB ENBL-N to go high which activates G33. The output of G33 resets FF9, TF11, and FF12. If the CCL and: RMR functions arc not requesting a level 2 interrupt INFIBUS access, and if the RSJ and

CCL functions are not requesting a direct memory access, shift register U4 continues to serially shift data, as explained previously

5-645. When the CCL function is requesting a level 2 interrupt INFIBUS access, operation is similar to when the RSJ is requesting a level 2 interrupt INFIBUS access except CCL INT REQ is high. This causes the same operations as when RSJ INT REQ was high, except G9 is enabled by the output of register U15 and activated when OD-N is low. Activating G9 causes shift register U4 to stop serially shifting data when OD-N is low. When FF2 is set G10 is activated which causes CCL INT ACK to go high. Also, the output of G9, R4-N, activates G16 which causes a request for a level 2 interrupt INFIBUS access to be generated, as explained previously.

5-646. When the RMR function is requesting a level 2 interrupt INFIBUS access, operation is similar to when the RSJ is requesting a level 2 interrupt INFIBUS access except RMR INT REQ is high. This causes the same operations as when RSJ INT REQ was high, except G11 is enabled by the output of register U15 and activated when OE-N is low. Activating G11 causes the shift register U4 to stop serially shifting data when OE-N is low. When FF2 is set, G12 is activated which causes RMR INT ACK to go high. Also, the output of G11, R5-N activates G16 which causes a request for a level 2 interrupt INFIBUS access to be generated, as explained previously.

5-647. If in the RSJ or CCL direct memory access operation or the RSJ, CCL, or RMR level 2 interrupt INFIBUS access operation the I/O Controller INFIBUS access logic circuit does not receive DONE-P within 2 USEC after STRB-N is generated, the Bus Controller generates QUIT-N. QUIT-N is inverted by inverter I23 which activates $\overline{\text{I/O QUIT}}$ G28. Activating G28 generates $\overline{\text{I/O QUIT}}$ for the duration of QUIT-N. The output of I23, QUIT-P, activates G33 (STRB ENBL-N low) which resets FF9, FF11, and FF12. Resetting FF9 removes STRB-N. Resetting FF11 disables G29 and resetting FF12 disables Gl which disables G4, G6, G8, G10, and G12.

5-648. PROGRAM MAINTENANCE PANEL ADDRESS/DATA SWITCH IDENTIFICATION, MULTIPLEXERS, AND LED CIRCUIT.

5-649. General. The Program Maintenance Panel address/data switch identification, multiplexers, and LED circuit provides identification of any address or data switch closure. It generates 16 shift pulses for serially loading either the address or data shift registers with the latest address or data information as determined by the address or data switch closures. It contains circuits to display either the address and data information as determined by the address or data switch closures or the address and data information from the data multiplexer and bus driver receiver circuit. The Program Maintenance Panel address/data switch identification, multiplexers, and LED circuits also provides circuits For serially incrementing the address shift register by one or two. Underscored names indicate front panel placarded nomenclature.

5-650. Detail Analysis (see figure 99). When OADS-P and ODAS-P are low and ENBL-N is low, both gates G3 and G4 are able to sink current through inductors Ll and L2, respectively, if an address or data switch is closed. When the address 15 switch (S21) is touched, current begins to flow from the output of G3, through L2, S21, and resistor R8. ENAD-N rises instantly to 5 volts and then decays to 0 volts in less than one msec. This positive differentiated voltage spike is coupled through driver DR2, differentiator L3 and R16, to trigger single shot SSl on its leading edge. The double differentiation is necessary to prevent oscillations between SSl and single shot SS2 after SSl or SS2 is triggered. When SS1 is triggered, OADS-P is generated for 3.55 msec. OADS-P causes the output of gate G2 to go low, forcing SS2 to remain cleared. OADS-P also causes the output of gate G4

to to high which prevents a data switch closure from being sensed during the **time** OADS-P is high. A data switch closure operates similarly to an address switch closure, except SS2 is triggered and the output of gate G3 is high for the duration of ODAS-P. This prevents an address switch closure from being sensed during the time ODAS-P is high. When FBAS-P from the Program Maintenance Panel switch flip-flops and single action discriminator circuit is generated, Gl and G2 are activated which holds SSl and SS2 cleared preventing either an address or data switch closure from being sensed.

5-651. Initially, MRES-N is inverted by I3 and I4. The output of I4, MREW-N, resets flip-flops FF2, FF3, and FF4 and single shot SS5. Resetting SS5 causes OLTS-P to hold flip-flop FFl reset. MREW-N activates G23 and G25 which resets address shift registers U58 and U78 and data shift registers U8 and U28. When O-ADS-P or ODAS-P goes high and if 7ACT-P and SWIT-P are low and RGSL-N is high, the output of gate G6 (waveform A, figure 100) goes low triggering single shot SS3. At the same time single shot SS5 is enabled to be triggered by the output of inverter I6. I6 inverts CLKI-N from the Program Maintenance Panel state generation and micro operations circuit. The output of I6 retriggers SS5 every 640 nsec. This causes OLTS-P to go high, enabling FFl to be set. The output of SS3 (waveform B, figure 100) returns to a high 1.9 msec after OADS-P or ODAS-P goes high, triggering single shot SS4 which generates OACS-P (waveform C, figure 100). The trailing edge of the low output of SS4 sets FFl which holds SS3 and SS4 cleared. OLTS-P (waveform D, figure 100) goes low 24 msec after the output of G6 returns to high. When OLTS-P goes low FFl is reset enabling SS3 and SS4 for the next switch closure.

5-652. If an address switch was touched, OADS-P enables gates G7 and G20. The output of G7 activates G11. FF4 IS set on the next negative going edge of the clock output of I6. The i output of FF4 enables gate GI2 to couple the clock output of I6 to inverter I5 and FF5. The I output of FF4 is coupled through inverter I7 and delay DL2. DL2 delays the positive going edge of FSAA-N only. The output of DL2, FSAA-N (waveform E, figure 100), enables address shift registers U58 and U78 to shift address information serially left (A15S-P to AOOS-P) when triggered by ASCA-N. The 0 output of FF4 enables the shift counter U12 to count. The gated clock pulses out of G12 (waveform F, figure 100) are inverted by I5 and activate gate G10 which triggers the shift counter U12. When shift counter U12 reaches the sixteenth count, G13 is activated. The output of G13 is inverted by inverter 18 and applied to the clear input of FF4. The next trailing edge of the clock output of I6 clears FF4 which clears shift counter U12 and disables G12. Disabling G12 causes FSAA-N to go high. The shift counter U12 generates BCD signals SC IS-P, SC2S-P, SC4S-P, and SC8S-P which are routed to the address/data bit multiplexer U50. Address/data bit multiplexer U50 converts the parallel inputs (only one input low) to a serial output. SCSl-P, SCS2-P, SCS4-P, and SCS8-P sequentially enables the EO through El5 inputs to the address/data bit multiplexer to be coupled to the output X as SMUX-P. This serial data, SMUX-P, activates G20 which activates gate G19. The output of G19, INAX-P, is routed to gate G22. The 16 ASCA-N pulses clock the serial address information bits, INAX-P, into address shift registers U58 and U78 for each address switch closure. The first address switch closure clocks the address information into the proper position of address registers U58 and U78. Assume address 15 switch is touched first, SMUX-P remains low until the shift counter U12 reaches count 16, SMUX-P then goes high. SMUX-P is coupled through G20, G19, and G22 to the shift left input of address shift register U58 and U78. ASCA-N is now at the sixteenth count and the address 15 information is stored in address shift registers U58 and U78. A15S-P goes high, is inverted by inverter I12 and causes the address 15 LED (CR21) to light. For each additional address switch closure the

above sequence is repeated and the address information stored in address shift registers U58 and U78 is circulated back to its original position through G22. If the address clear switch (S37) is touched, the address clear LED (CR37) lights and SCLA-N activates G23 which resets address shift registers U58 and U78. If an address switch is touched a second time, the associated bit position in address shift registers U58 and U78 is cleared. If the address 15 switch is touched a second time, the above sequence is repeated except; at the sixteenth ASCA-N clock pulse AOOS-P and INAX-P are both high. The output of G22 is low and a 0 is clocked into bit position 15 of address shift registers U58 and U78 which causes the address 15 SLED to go out.

5-653. To increment address shift registers U58 and U78 by one, FF3 is preset by FSAT-N from the Program Maintenance Panel state generation and micro operations circuit and lPNC-N presets FF5. Setting FF3 sets FF4 on the next trailing edge of the clock pulse out of I6. Setting FF4 enables shift counter U12 and address registers U58 and U78, as explained previously. The shift counter generates the BCD signals SC15-P, SC2S-P, SC4S-P, and SC8S-P and the 16 ASCA-N pulses, as explained previously. BYSW-N is low when address shift registers U58 and U78 are to be incremented by one. BYSW-N is inverted by I9 which enables G25 and G17. The 1 output of FF5 activates G17 which activates G20 holding INAX-P high. When INAX-P and AOOS-P are high, G22 functions as a half adder and a 0 is clocked into the associated bit position of address shift registers U58 and U78 where a 1 was stored. INAX-P remains high until AROO-N goes high, which corresponds to a 0 in associated address shift registers U58 and U78 bit position. When AROO-N goes high G15 is activated which activates G16. On the next negative going edge of the clock pulse out of G12, a 1 is clocked into address shift registers U58 and U78. This occurs because INAX-P is still high, incrementing the address in **address** shift registers U58 and U78 by one. FF5 is cleared on the second negative going edge of the clock pulse out of G12 which disables G18. The output of G18 disables G19 which causes INAX-P to go low. The information remaining in the address shift register is circulated, as explained previously, by the ASCA-N pulses until shift counter U12 reaches a count of 16. When a count of 16 is reached, G13 is activated. The output of G13 is inverted by I8 which resets FF3 and FF4. Resetting FF3 and FF4 clears shift counter U12 and disables address shift registers U58 and U78.

5-654. To increment address shift registers U58 and U78 by two is similar to incrementing the address shift register by one, except BYSW-N is high. BYSW-N is inverted by I9 which disables G15 and G18 and enables G17. The output of G14 is high at **a** count of 0 which disables G17. The output of G14 is also inverted by inverter I/O which disables G5. After the first count, the output of G14 goes low activating G18 and is inverted by I10 which enables G15. Activating G18 activates Cl7 causing INAX-P to go high for the second and following counts. When INAX-P and AOOS-P are high, G22 functions as a half adder and a 0 is clocked into the associated position of address shift registers U58 and U78 where a 1 was stored. INAX-P remains high until AROO-N goes high which corresponds to a 0 in associated address shift registers U58 and U78 bit position. When AROO-N goes high, G15 is activated which activates G16. On the next negative going edge of the clock pulse out of G12, a 1 is clocked into address shift registers U58 and U78 because INAX-P is still high. This increments address shift registers U58 and U78 by two because the 0 bit position of **the** address shift register was skipped by the action of G14. The remaining address shift registers U58 and U78 information is circulated, the shift ***counter*** U12 is cleared and the address shift register is disabled as explained previously.

5-655. When PSAA-N is high address shift registers U58 and U78 can accept the 16-bit parallel address information DOOA-P through D15A-5 from the Program Maintenance Panel data multiplexer and bus

driver receiver circuit. The 16-bit parallel address information is clocked into address shift registers U58 and U78 by ASCA-N which at this time is the ASCB-N signal from the Program Maintenance Panel INFIBUS access circuits.

5-656. If a data switch was touched, ODAS-P enables and G21. G8 is activated 1.9 msec after ODAS-P is generated, as explained previously. The output of G8 (waveform C, figure 100) is applied to flip-flop FF2. FF2 is set on the next negative going edge of the clock output of I6. The 1 output of FF2 is inverted by inverter I2. The output of I2 is applied to DLl which delays the positive going edge of FSDA-N only. The output of DLl, FSDA-N (waveform E, figure 100), enables data shift registers U8 and U28 to shift data information serially left (D15S-P to DS-P) when triggered by DSCA-N. The 1 output of FF2 enables gate G9 to couple the clock output of I6 to G10 and data shift registers U8 and U28. The 0 output of FF2 enables shift counter U12. The gated clock pulses out of G9 (waveform F, figure 100) are coupled through G10 to trigger shift counter U12. When shift counter U12 reaches the sixteenth count, G16 is activated. The output of G16 is inverted by I8 and applied to the clear input of FF2. The next trailing edge of the clock output of I6, clears FF2 which clears shift counter U12 and disables G9 causing FSDA-N to go high. The shift counter U12 generates BCD signals SClS-P, SC2S-P, SC4S-P, and SC8S-P which are routed to address/data bit multiplexer U50. Address/data bit multiplexer US 0 converts the parallel inputs (only one low) to a serial output as strobed by the outputs of shift counter U12 for each data switch closure. This serial data, SMUX-P, activates gate G21. The output of G21 is inverted by I11. The output of Ill, DMUX-P, is routed to gate G24. The 16 DSCA-N pulses clock the serial data information bits, DMUX-P, into data shift registers U8 and U28 for each data switch closure. The first data switch closure clocks the data information into the proper position of data registers U8 and U28. If data 15 switch is touched first, SMUX-P remains low until the shift counter U12 reaches count 16, S MUX-P goes high which activates G21. The output of G21 is inverted by Ill which activates G24. DSCA-N is now at the sixteenth pulse and the data 15 information is stored in data shift registers U8 and U28. Al5S-P goes high, and is inverted by inverter I14 which causes the data 15 LED (CR44) to light. For each additional data switch closure the above sequence is repeated and the data information stored in data shift registers U8 and U28 is circulated back to its original position by G24. If the data clear switch (S55) is touched, the data clear LED (CR56) lights and G25 is activated which resets data shift registers U8 and U28. If a data switch is touched a second time, the associated bit position in data shift registers U8 and U28 are cleared. If data 15 switch is touched a second time, the above se-- quence is repeated except at the sixteenth DSCA-N clock pulse DOOS-P and DMUX-P are both high. The output of G24 is low and a 0 is clocked into bit position 15 of data shift registers U8 and U58 which causes the data 15 LED to go out.

5-657. When 7ACT-P from the Program Maintenance Panel switch flip-flops and single action discriminator circuit is generated, it is inverted by inverter I1 which activates G5. The output of G5 activates G6 which causes OACS-P and OLTS-P to be generated, as explained previously. If RGSL-N goes low, G5 is activated which causes OACS-P and OLTS-P to be generated. If SWIT-P from the Program Maintenance Panel miscellaneous control circuit goes high, G6 is activated and OACS-P and OLTS-P are generated, as explained previously. However, because OADS-P and ODAS-P are low shift counter U12 and address shift registers U58 and U78 or data shift registers U8 and U28 are not enabled.

5-658. PROGRAM MAINTENANCE PANEL CPU REGISTER SELECTION CIRCUIT.

5-659. General. The Program Maintenance Panel CPU register selection circuit converts the CPU register selection switch closure to a 4-bit BCD signal that is routed to the Program Maintenance Panel address multiplexer, bus driver receiver, and recog-

nition circuit. The CPU register selection circuit also displays the number of the CPU register selected.

5-660. Detail Analysis (see figure 101). Initially, MRE-N from the Program Maintenance Panel address/data switch identification multiplexer, and LED circuit resets the CPU selection storage register U62. When register 15 switch (S2) is touched, RS15-P goes high and is routed to the decimal-to-BCD encoder U52. When RS15-P goes high the four outputs (01 through 04) and the STRB output of decimal-to-BCD encoder U52 goes low generating RGSL-N which is routed to the Program Maintenance Panel address/data switch identification, multiplexers, and LED circuit. Inverter I2 enables gate Gl and RGSL-N is inverted by inverter I1, also enabling Gl. 1.9 msec after RGSL-N goes low, OACS-P from the Program Maintenance Panel address/data switch identification, multiplexers, and LED circuit is generated for 3.4 msec which activates Gl. The delayed 3.4 msec pulse out of Gl clocks the four high outputs (01 through 04) of decimal-to-BCD encoder U52 into CPU selection register U62. The four outputs (RAO1-N through RA04-N) of CPU selection register U62 are routed to the Program Maintenance Panel address multiplexers, bus driver receiver, and recognition circuit. The other four outputs, QAl through QDl, of CPU selection register U62 are routed to the BCD-to-decimal decoder U72, generating R15L-N which lights the reqister 15 LED (CR2). If two register switches are touched simultaneously, the KRO output of the decimal-to-BCD encoder U52 goes low which disables Gl. Disabling G1 prevents the 01 through 04 outputs of decimal-to-BCD encoder U52 from being clocked into CPU selection register U62.

5-661. PROGRAM MAINTENANCE PANEL ADDRESS MULTIPLEXER, BUS DRIVER RECEIVER, AND RECOGNITION CIRCUIT.

5-662. General. The Program Maintenance Panel address multiplexer, bus driver receiver, and recognition circuit strobes either the address information from the Program Maintenance Panel address/data switch identification, multipiexers, and LED circuit, the CPU register address information from the CPU register selection circuit, or the CPU control register address information to the INFIBUS address lines. The address multiplexer, bus driver receiver, and recognition circuit also notifies the Program Maintenance Panel state generation and micro operations circuits when the address on the INFIBUS equals the address selected by the Program Maintenance Panel address/data switch identification, multiplexers, and LED circuit. These circuits also indicate when the INFIBUS is busy and notify the Program Maintenance Panel state generation and micro operations circuit when the Program Maintenance Panel address is on the INFIBUS address lines.

5-663. Detail Analysis (see figure 102). When ARAB-P and CRAB-N are high (address register selection), gates G2, G3, G4 and G5 are enabled and AOOS-P through A15S-P are coupled through the address multiplexers U46, U56, U66 and U76. When AOUT-P goes high the inputs are strobed through address bus driver receivers U50, U60, U70 and U80. The information on the INFIBUS, ABOO-N through AB15-N, either from the INFIBUS or address bus driver receivers U50, U60, U70, and U80 is coupled through address bus driver receivers U50, U60, U70, and U80 to the address exclusive-nor gates U47, U57, U67, and U77. If AOOS-P through Al5S-P equals AOOA-P through Al5A-P, the output of address exclusive-nor gates U47, U57, U67 and U77 is high. If address bit 15 (A15S-P) in the address shift register of the Program Maintenance Panel address/data switch identification, multiplexers, and LED circuit is high, the output of the address multiplexer U46 is low, enabling gate Gl. When AOUT-P goes high, Gl is activated and ABl5-N goes low. ABl5S-N is inverted by inverter I1 (Al5A-P goes hiqh). With A15A-P and A15S-P both high, the output of gate G6 is high, enabling gate G7. STRB-N is inverted by inverter 12 and gate G7 is activated 50 msec after STRB-N goes low by the delay of DLl, causing EQA4-P

to go high. The output of I2 is also routed to SS1. As long as SS1 is being triggered at least once every 0.088 sec, its output remains high. This high level output of SSl is inverted by inverter I3, which causes the busy LED (CR39) to light. When STRB-N remains high for longer than 0.088 sec the output of SSl returns to a low level and the busy LED goes out.

5-664. When ARAB-P is low and CRAB-N is high (CPU register selection), the 0 volt, +5 volts, CPUO-N and CPUl-N (both high) and RAl-N through RAl-N inputs are coupled through address multiplexer U46, U56, U66, and U76. G2, G3, G4, and G5 are enabled by CRAB-N being high and the outputs of address multiplexer U46, U56, U66, and U76 and G2, G3, G4, and G5 are strobed through bus driver receivers U50, U60, U70, and U80 when AOUT-P goes high. For this condition AB15-N through AB08-N are low, AB07-N, AB06-N, AB05-N, and ABOO-N are high, and the selected CPU register address is /1,1,1,1, /1,1,1,1, /0,0,0, RAO4-N, / RA03-N, RA02-N, RA0l-N, O/. A15A-P through AOOS-P now does not equal A15S-P through AOOS-P and the output of the exclusive-nor gates U47, U57, U67, and U77 is not high and EQA4-P is not generated.

5-665. When ARAB-P and CRAB-N are low (CPU control register selection) the 0 volt, +5 volts, CPUO-N and CPUl-N (both high) and the RA04-N through RAOl-N inputs are coupled through address multiplexer U46, U56, U66 and U76. G2, G3, G4, and G5 are disabled (output low) by CRAB-N being low and the outputs of address multiplexer U46, U56, U66, and U76 and G2, G3, G4, and G5 are strobed through bus driver receivers U50, U60, U70 and U80 when AOUT-P goes high. EQA4-P is not generated, as explained previously.

5-666. When the Program Maintenance Panel is operating in the slave mode (being addressed by another module), gates G8, G9, G10, G11, G12, G13, and G14 and inverters I6, I7, and I8 determine when the Program Maintenance Panel address, FF8X (/1111/1111/1000/01XX/), is on the INFIBUS address lines. HCYC-N is high which is inverted by inverter I9, which activates gate G14. PBOO-N and PB0l-N are always low, and if Al5A-P through A07A-P are high, and A06A-P through A02A-P are low, the junction of the outputs of G9, G10, G11, G12, G13, G14, I5, I6, I7 and I8 remains low until the output of I2 goes high. Delay DL2 delays the positive going edge of the output of G8, G9, G10, G11, G12, G13, G14, I5, I6, I7 and I8 to prevent false address recognition. The output of DL2 is inverted by inverter I4. This causes SARO-N to go low which notifies the Program Maintenance Panel state generation and micro operations circuit that address recognition has occurred.

5-667. PROGRAM MAINTENANCE PANEL DATA MULTIPLEXER AND BUS DRIVER RECEIVER CIRCUIT.

5-668. General. The Program Maintenance Panel data multiplexer and bus driver receiver circuit can couple the address or data information from the Program Maintenance Panel address/data switch identification, multiplexer, and LED circuit to the INFIBUS and couple data information from the INFIBUS to the address/data switch identification, multiplexer, and LED circuit. The Program Maintenance Panel data multiplexer and bus driver receiver circuit can also couple either the halt command, run command, step command, zero address, or Program Maintenance Panel address to the INFIBUS.

5-669. Detail Analysis (see figure 103). The address shift register outputs, AOOS-P through A15S-P, from the Program Maintenance Panel address/data switch identification, multiplexer, and LED circuits are coupled through the data multiplexers U6, U16, U26 and U36 when DRDB-N is high and RNDB-P, VADB-P, and HTDB-P are low. When VADB-P is low, gates G2 through G10 are enabled. When RNDB-P and HTDB-P arc low gates G13 and G14 are enabled. With both RNDB-P and VADP-B low, gate G15 is disabled (output high). The low level of HDTB-P is inverted by inverter I7. The high outputs of gate G15 and inverter

I7 disable gate G16 (output low). The low outputs of inverters I5 and I6 are constantly disabling the lower AND gates of gates G11 and G12 causing G11 and G12 to function as inverters. When DRDB-N is high the low output of G16 strobes the AOOS-P through Al5S-P inputs through data multiplexers U6, U16, U26, and U36. The outputs of data multiplexers U6, U16, U26, and U36 are coupled through enabled gates G2, G3, G4, G5, G6, G7, G8, G9, G10, G11, G12, G13, G14 and inverters I2, I3 and I4 to the bus driver receivers U10, U20, U30, and U40. When DOUT-P goes high, the 16-bit data information is strobed through the data bus driver receivers Ul0, U20, U30, and U40 to the INFIBUS and inverted and routed to the address and data shift registers of the Program Maintenance Panel address/data switch identification, multiplexers, and LED circuits. For example, assume A15S-P is high, the high 4Y output of data multiplexer U6 is coupled through and inverted by enabled G2 to gate Gl. When DOUT-P goes high Gl is activated and DBl5-N goes low. Also, data signals from the infibus are coupled through the inverters of data bus driver receivers Ul0, U20, U30, and U40 to the address and data shift registers of the Program Maintenance Panel address/data switch identification, multiplexers, and LED circuits.

5-670. The data shift register outputs, DOOS-P through Dl5S-P, from the Program Maintenance Panel address/data switch identification, multiplexer, and LED circuits are coupled to the INFIBUS when DRDB-N, RNDB-P, VADB-P, and HTDB-P are low. Operation is similar to the address shift register outputs, AOOS-P-A15S-P, except DRDB-N is low, the output of Gl6 couples the DOOS-P through Dl5S-P inputs through data multiplexers U6, U16, U17 U18.

5-671. The halt command /l, 1, 1, 1, /1,1,1,1,/1,1,1,1,/1,1,0/ (0001 16) is strobed to the INFIBUS by DOUT-P when RNDB-P and VADB-P are low and HTDB-P is high. HTDB-P IS inverted by I7 and the low output of 17 activates G16. The high output of G16 forces all of the data multiplexers U6, U16, U26 and U36 outputs low. With VADB-P low, G2 through G10 are enabled. With HTDP-P high, G14 is activated and its low output is applied to the DBOO-N input of data bus driver receiver U40. G13 is disabled by RNDB-P (low). The outputs of G2 through G13 and 12, I3, and I4 are now high and the output of G14 is low. When DOUT-P goes high the halt command is strobed to the INFIBUS as explained previously.

5-672. The runcommand /l,l,l,l, /1,1,1,1,/i,i,1,1,/1,1,0,1/(000216) is strobed to the INFIBUS by DOUT-P when RNDB-P is high and VADB-P and HTDB-P are low. The high level of RNDB-P is inverted by G15, forcing the output of G16 high. The high output of G16 forces all of the data multiplexers U6, U16, U26, and U36 outputs low. With VADB-P low, G2 through G10 are enabled. RNDB-P activates G13, forcing its output low. With both inputs to G13 low, its output is high. The outputs of G3 through G12, G14, and I2, I3, and I4 are now high and the output of G14 is low. When DOUT-P goes high the run command is strobed to the INFIBUS, as explained previously.

5-673. The step command /l,l,l,l, /1,1,1,1,/1,1,,1,/1,1,0,0,/(0003 16) is strobed to the INFIBUS by DOUT-P when RNDB-P and HTDB-P are high and VADB-P is low. Operation is similar to the halt and run commands, as explained previously, except the outputs of G13 and G14 are both low due to RNDB-P and HTDB-P, respectively.

5-674. The zero address /l,1,1,1, /1,1,1,1,/1,1,1,1,/1,1,1,1/(000016) is strobed to the INFIBUS by DOUT-P when RNDB-P, VADB-P, HTDB-P and FMRA-N are low. Operation is similar to when the address shift register or data shift register information is strobed to the INFIBUS, except the **output** of G16 is held high by FMRA-N, forcing all of the outputs of data multiplexers, U6, U16, U26, and U36 low.

5-675. **The control panel address** /0,0,0,0, /0,0,0,0,/0,1,1,1,/1,1,1,1,/(FF80 16)

is strobed to the INFIBUS by DOUT-P when RNDB-P and HTDB-P are low and VADB-P is high. Operation is similar to when the address shift register or data shift register information is strobed to the INFIBUS, except the output of G16 is held high by VADB-P via G15, forcing all outputs of data multiplexers U6, U16, U26, and U36 low. The high level of VADB-P also forces the outputs of G12 through G10 low, overriding the low outputs of data multiplexers U6, U16, U26, and U36. When DOUT-Pgoes high the Program Maintenance Panel address is strobed to the INFIBUS.

5-676. PROGRAM MAINTENANCE PANEL SWITCH FLIP-FLOPS AND SINGLE ACTION DISGRIMINATOR CIRCUIT.

5-677. General. The Program Maintenance Panel switch flip-flops and single action discriminator circuit detects the closure of either the run, halt, step, address read, address write, resister read, or resister write switches and clock this information into the switch registers. If two switches are touched at the same time, information is not clocked into **the** switch flip-flops. These circuits also disable the address and data 00 through 15 switches.

5-678. Detail Analysis (see figure 104). Initially, MREU-N activates gate G17 which resets flip-flop FF2. If run switch (S58) is touched, the output of inverter I1 goes high. The output of I1 is coupled through gate G1 to the switch flip-flops (FFl shown) and through gates G2, G4, G5, G6, G7, and G8 causing 7ACT-P to go high which enables gate G15. 1.9 msec after 7ACT-P goes high, OASC-P goes high for 3.4 usec, activating G15 which sets FF2 when OACS-P goes low. Setting FF2 causes single shot SSl to generate a 3.4 **usec** pulse **that** sets FFl. 7ACT-P also activates gate G18 which enables gate G19. OACS-P activates Gl9 for 3.4 uscc, 1.9 msec after 7ACT-P goes high. The delayed 3.4 usec pulse, ANRW-N, is routed to the Program Maintenance Panel state generation and micro operations circuit. When FF2 is set, PBAS-P is high and is routed to the Program Maintenance Panel switch identification, multiplexers, and LED circuit to disable the address and data 00 through 15 switches.

5-679. If the halt switch (S59) is touched, the output of inverter I2 goes high. The output of I2 is coupled through G-3 to the switch flip-flops and through G2, G4, G5, G6, G7, and G8, causing 7ACT-P to go high. The associated switch flip-flop is set and ANRW-N is generated, as explained previously.

5-680. If the step switch (S61) is touched. the step LED (CR64) lights and the output of inverter I3 goes high. The output of I3 is coupled through Gl and G3 to the switch flip-flops and through G4, G5, G6, G7 and G8 causing 7ACT-P to go high. Two switch flip-flops are set and ANRW-N is generated, as explained previously.

5-681. If the address read switch (S38) is touched, the address read LED (CR38) lights and the output of inverter I4 goes high. The output of I4 is routed to the switch flip-flops and coupled through G5, G6, G7 and G8, causing 7/ACT-P to go high. The associated switch flip-flop is set, as explained previously. The output of I4 also activates gate G16, which disables G19, preventing ARNW-N from being generated.

5-682. If the address write switch (S20) is touched, the address write LED (CR20) lights and the output of inverter I5 goes high. The output of I5 is routed to the switch flip-flops and coupled through G6, G7 and G8, causing 7ACT-P to go high. The associated switch flip-flop is set, as explained previously. The output of I5 also activates G16 which disables G19, preventing ANRW-N from being generated.

5-683. If the register read switch (S19) is touched, the output of inverter I6 goes high. The output of I6 is routed to the switch flip-flops and coupled through G7 **and G8, causing 7ACT-P to go high. The** associated switch flip-flop is set and **ANRW-N** is generated, as explained previously.

5-684. If register write switch (S1) is touched, the output of inverter I7 goes high. The output of I7 is routed to the switch flip-flops and coupled through G8, causing 7ACT-P to go high. The associated switch flip-flop is set and ANRW-N is generated, as explained previously.

5-685. OA1G-P resets the switch flip-flops and OFBA-N activates G17 to reset FF2 when the transfer is completed.

5-686. OACS-P and SWIT-P go high when the reset, load, adh, or attn switch on the Program Maintenance Panel miscellaneous control circuit is touched. OACS-P enables G19 and SWIT-P activates G18 which activates G19.

5-687. If two or more of the switches are touched simultaneously, the outputs of two or more inverters go high which activates one or more of gates G9, G10, G11, G12, G13, or G14. OACS-P is generated as explained previously and FF2 is clocked, but remains cleared. If the halt switch and register write switch are touched simultaneously, the output of I2 goes high and is coupled through G2, G4, G5, G6, and G7, enabling G14 and the output of I7 goes high activating G14, causing its output to go low which prevents FF2 from setting.

5-688. PROGRAM MAINTENANCE PANEL MISCELLANEOUS CONTROL CIRCUIT.

5-689. General. The Program Maintenance Panel miscellaneous control circuit allows an autoload signal to be generated, by the load switch closure, after a master reset has been generated. The miscellaneous control circuit also generates the master inhibit pulse, which is routed to the INFIBUS and causes the Program Maintenance Panel to generate the halt command when the adh switch is touched. These circuits also cause a level 1 interrupt to be generated when the attn switch is touched. These circuits also control the status of the load, inh, adh, reset, run, idle, and halt LEDS.

5-690. Detail Analysis (see figure 105). When the Program Maintenance Panel state generation and micro operations circuit receives a master reset pulse, MRES-N, MREU-N goes low. MREU-N resets FF1, FF2, and FF3. Inverter I2 constantly enables gate G1 which is activated when FFI resets, The output of G1 enables gate G2 and is coupled through driver DR1 causing AULL-N to go low which lights the load LED (CR59). When the load switch (S57) is touched, SLOD-N goes low activating G2. The output of G2 activates gate G4 and enables gate G3. The output of G4 is inverted by inverter I9 causing SWIT-P to go high. 1.9 msec after SWIT-P goes high, OACS-P goes high for 3.4 usec and is inverted by inverter I8. The output of I8 activates G3 and enables G6. The output of G3 is coupled through driver DR2 causing ATLD-N (autoload) to go low for 3.4 usec. At the end of any INFIBUS transfer, DONF-P from the Program Maintenance Panel INFIBUS access circuit goes high and is inverted by inverter I1. The out put of I1 presets FFl which disables G1, causing the load LED to go out and prevents any further load switch closures front generating ATLD-N until another master reset pulse is generated on the INFIBUS.

5-691. When the inh (inhibit) switch S62 is touched, SIN11-N goes low and is inverted by inverter I4. The high output of I4 remains high as long as the inh switch is touched and is routed to FF2. SINH-N also activates G4 which causes SWIT-P to be generated. 1.9 mscc after SWIT-P goes high, OACS-P goes high for 3.4 usec. The trailing edge of OACS-P sets FF2 and ensures FF3 is cleared. The output of FF2 is inverted by inverter I3 causing FITL-N to go low, lighting the inhD (CR65). The output of FF2 is also Inverted by inverter I5 causing MINH-N to go low, FF2 remains set until an MRCU-N pulse is *received* or another switch closure generates OACS-P.

5-692. When the adh switch S60 is touched, SADH-N goes low which activates G4. This causes SWIT-P to be generated as explained previously.

msec after SWIT-P goes high OACS-P goes high. SADW-N is also inverted by inverter I6. The output of I6 is routed to FF3 and the trailing edge of OACS-P sets FF3 and ensures FF2 is cleared. The output of FF3 is inverted by inverter I7 causing FAHL-N to go Bow, lighting the ad& LED (CR63). The output of FF3, FAHS-P, is also routed to the Program Maintenanc Panel state generation and micro operations circuit which causes the address halt command to be strobed to the INFIBUS data lines and the CPU conntrol register address to be strobed to the INFIBUS address lines when INFIBUS access is gained (when address on INFIBUS equals address in address shift register. FF3 remains set until an MREU-N pulse is received or another switch closure causes OACS-P to be generated.

5-693. Whew the attn (attention) switch is touched, SATN-N goes low and is coupled through driver DR3. The low output of DR3 enables gate G6 and activates gate G5. The output of G5 activates G4 ad the output of G4 is inverted by I9 causing SWIT-P to go high. When SWIT-P goes high OLTS-P goes high and 1.9 msec after SWIT-P goes high OACS-P goes high for 3.4 usec. OACS-P is b-averted by I8 which activates G6. This low output of G6 presets flip-flop FF-4 causing FTTR-N to go low. 24 msec after the attn switch is released, OLTS-P returns to a low level which resets FF4 causing FTTR-N to return to a high level. This Bow-to-high level transistion of FTTR-N causes the Program Maintenance Panel INFIBUS access circuit to generate a level 1 interrupt.

5-694. When the reset switch S56 is touched, SRST-N goes low and is routed to the INFIBUS as REPB-N which causes a master reset pulse, MRES-N, to be generated by the Bus Controller. SET-N is also coupled through driver DR4 and DR5 causing REPL-N to go low which causes the reset LED (CRS8) to light for as long as the reset switch is touched. The low output of DR4 also activates G5 which causes SWIT-P to bc generated, as explained previously.

5-695. When SRLC-N goes low, the output of inverter I10 goes high which causes the output of inverter I11 to go low. The output of I11 is delayed 11 usec by delay DL1. The output of DL1 is inverted by inverter I12. This high output of I12 is inverted by inverter I13 causing RUNL-N to go low which causes the run LED (CR60) to light. When SRLC-N returns to high, the output of DL1 goes high after 11 usec (if SRLC-N does not go low again). This high output of DL1 is inverted by I12 which activates gate G7 if RUNN-N is low. Activating G7 causes IDLL-N to go low which lights the idle LED (CR61). The output of I12 is also inverted by I13 which causes the run LED (CR60) to go out. If two or more SRLC-N pulses are received within 11 usec, the output of DL1 does not go high and the run LED remains lighted and the idle LED remains not lighted. As long as RUNN-N pulses are received within 120 msec, the output of single shot SS1, which is triggered by CLQP-P, remains low. This low output of SS1 is inverted by inverter I14. The high output of I14, ORNL-P, prevents the halt LED (CR62) from lighting. When RUNN-N remains high for more than 120 msec, the output of SS1 goes high which is inverted by I14. This low output of I14 causes the halt LED to light until 120 msec after RUNN-N goes low again.

5-696. PROGRAM MAINTENANCE PANEL STATE GENERATION AND MICRO OPERATIONS CIRCUIT.

5-697. General. The Program Maintenance Panel state generation and micro operations circuit determines which address information and data information is strobed to the INFIBUS lines. The Program Maintenance Panel state generation and micro operations circuit causes the halt, run, or step command to be routed to the CPU control register, causes the displayed data to be routed to the displayed address or the displayed register, or causes the data from the displayed address or the displayed register to be displayed. The Program Maintenance Panel state generation and micro operations circuit also causes the halt command to be strobed to the INFIBUS if the address halt, adh, switch has been touched when the address on the INFIBUS address lines is the same as the address

determined by the address 0 through 15 switches. This circuit also causes the Program Maintenance Panel address to be strobed to the INFIBUS during a level 1 interrupt. In the slave mode (when being addressed by another function) this circuit causes either the address or data switch closure information to be strobed to the INFIBUS lines.

5-598. Detail Analysis (see figure 106). Initially, MRES-N is coupled through inverter I6. The output of I6 activates gate G7 which resets flip-flop FF4. The output of I6 is also inverted by inverter I5 which resets flip-flops FFl, FF2, FF3, FF5, FF6, FF7, FF8, FF9, FF10, and FF11, state generator U34 and counter U55. MRBA-N, from the Program Maintenance Panel address/data switch identification, multiplexers, and LED circuit, goes low whenever a master reset, MRES-N, is received by the Program Maintenance Panel or when the address clear switch is touched. SFSA-N from the Program Maintenance Panel address/data switch identification, multiplexers, and LED circuit, goes low whenever an address 0 through 15 or data 0 through 15 switch is touched. ANRW-N from the Program Maintenance Panel switch flip-flops and single action discriminator circuit goes low whenever the run, halt, step, register read, or register write switches are touched. If MRBA-N or SFSA-N goes low, gate G24 is activated. The output of G24 is inverted by inverter I13. When the output of I13 or ANRW-N goes low, gate G25 is activated which sets flip-flops FF12 and FF13.

5-699. The 25 MHZ clock, CLKA-N, from the INFIBUS IS inverted by inverter I7 which constantly triggers counter U55. The divide by 4 output of counter U55, IS divided by 2 by FF6. The outputs of FF6 alternately enable gates G8 and G9 which are activated by the divide by 4 output of counter U55. The output of G9, CFOA-P (waveform: A, figure 107), and the output of G8, CFIA-P (waveform B, figure 107), are used to time operations in the state generation and micro operations circuit. The divide by 16 output of counter U55, CLOD-P, IS used to clock the Program Maintenance Panel miscellaneous control circuit. The divide by 16 output of counter U55 is also inverted by inverter I8, generating CLKI-N which clocks the Program Maintenance Panel address/data switch identification, multiplexers, and LED circuit.

5-700. Approximately 1.9 msec after the halt switch on the Program Maintenance Panel switch flip-flops and single action discriminator circuit is touched, OSTS-P goes high for 3.4 usec and FHTS-P goes high and FHTR-N go low. The trailing edge of OSTS-P (waveform C, figure 107) sets FF4 (waveform D, figure 107). Inverter I3 inverts the CFOA-P pulses. The first positive going edge out of I3, after OSTS-P goes low, triggers the state generator U34 causing FSAS-P (waveform E, figure 107) to go high and FSAT-N to go low. When FSAS-P goes high, G7 is activated which resets FF4. FSAS-P also clears FF11 if it was set. FSAT-N causes FSHR-N (waveform F, figure 107) to go low for 10.25 usec to allow for possible address register incrementation. The second positive going edge out of I3, triggers the state generator U34 a second time causing FSAS-P to go low and FSAT-N to go high. When FSHR-N goes high, FF3 is set, activating G4 which activates G5. The next positive going edge out of I3 triggers state generator U34, causing FSBS-P (waveform G, figure 107) to go high and FSBR-N to go low via inverter I2. The output of I2 presets FF5 which disables G5. The positive going edge out of I3, after FF5 is preset, triggers state generator U34 causing FSBS-P to go low and FSBR-N to go high.

5-701. While FSBS-P is high and FSBR-N is low, OFDN-N, lFND-N, and FWlS-P are genera ted. OFDN-N (waveform H, figure 107) is generated when FSBR-N activates gate G38 which enables G39. G39 is activated by CFlA-P. Gate G32 is enabled by FSPS-P and activated by CROA-P which activates gate G33. The outputs of G39, OFDN-N, and G33, lFND-N (waveform I, fIgure: 107) are routed to the Program Maintenance Panel INFIBUS access circuit to gain access to the INFIBUS. FSBS-P enables

gates G11, G13, G15, G17, and G18. CFIA-P activates G15 which ensures FF8 is cleared. CFOA-P activates gates G11 and G16, The output of G16 activates G17 which clears FF10 if it was set. The output of G11, IFW1-N (waveform J, figure 107), presets FF2 causing FWlS-P (waveform L, figure 107) to go high. FHTR-N activates gates G57 and G58. The output of G57 enables G51 and the output of G58 enables G59. When FWlS-P goes high, gates G51 and G59 are activated causing HTDB-P to go high and CRAB-P to go low. With ARAB-P and CRAB-N low, the CPU control register address is strobed to the INFIBUS address lines when infibus access is gained With HTDB-P high and RNDB-P and VADB-P low, the halt command is strobed to the INFIBUS data lines when INFIBUS access is gained.

5-702. When the Program Maintenance PaneI INFIBUS access circuit receives DONE-N or QUIT-N from the CPU, FDNR-N or FATR-N goes low. FDNR-N or FATR-N activates gate G3 which activates gate G2. The next positive going edge out of I3, after FDNR-N or FATR-N goes low, triggers state generator U34 which causes FSCS-P (waveform M, figure 107) to go high. FSCS-P activated gates G27 and G40. The output of G40 is inverted by inverter I15 causing OFWl-P (waveform N, figure 107) to go high which clears FF2 and ensures FF1 is cleared. The output of FF2 now disables G2 and the next positive going edge out of I3 causes FSCS-P to go low. The output of G40 also activates G38 which enables G39 to be activated by CFIA-P. The output of G39, the second OFDN-N pulse is routed to the Program Maintenance Panel INFIBUS access circuit. The output of gate G27 activates gate G28 which activates gate G29. The output of G29 is routed to gate G30. FDNS-P also goes high when DONE-N is received by the Program Maintenance Panel INFIBUS access logic circuit which enables G30. G30 is activated by CF1A-P causing IFAD-N to go low for one CF1A-P pulse. IFAD-N sets FF10. The output of FF10 is inverted by inverter I11, causing BADE-N to go low which lights the done LED CR57. FF10 remains set until a master reset pulse, MRES-N, is received by Program Maintenance Panel state generation and micro operations circuit or until FSBS-P is generated again which will only occur with another switch closure on the Program Maintenance Panel switch flip-flops and single action discriminator circuit. Because state generator U34 is now in its quiescent state (all outputs low), all operations in the state generation and micro operations circuits cease until the run or step switch on the Program Maintenance Panel switch flip-flops and single action discrimination circuit is touched.

5-703. When the run switch on the Program Maintenance Panel switch flip-flops and single action discriminator circuit is touched, operation is similar to when the halt switch is touched, except when OSTS-P goes high, FRNS-P goes high and FRNR-N goes low. FRNR-N activates G58 which enables gate G59 and FRNS-P enables gate G49. When FWlS-P goes high, gates G49 and G59 are activated causing RNDB-P to go high and CRAB-N to go low. With ARAB-P and CRAB-N low, the CPU control register address is strobed to the INFIBUS address lines when INFIBUS access is gained. With RNDB-P high and VADB-P and HTDB-P low, the run command is strobed to the INFIBUS data lines when INFIBUS access is gained. All operations are the same as when the halt switch is touched, except the Program Maintenance Panel state generation micro operations circuit remains in the quiescent state until OSTS-P is generated by another switch closure on the Program Maintenance Panel switch flip-flops and single action discriminator circuit, an address halt is required, or an address recognition occurs.

5-704. Approximately 1.9 msec after the step switch on the Program Maintenance Panel switch flip-flop and single action discriminator circuit is touched, OSTS-P goes high for 3.4 usec, FRNS-P and FHTS-P go high and FRNR-N and FHTR-N go low. The trailing edge of OSTS-P sets FF4. Inverter I3 inverts the CFOA-P pulses. The first positive going edge out of I3, after OSTS-P goes low,

triggers state generator U34 causing FSAS-P to go high and FSAT-N to go low. When FSAS-P goes high, G7 is activaated which resets FF4. FSAS-P also clears FF11 if it was set. FSAT-N causes FSHR-N to go low for 10.25 usec to allow for possible address register incrementation The second positive going edge out of I3, triggers state generator U34 a second time causing FSAS-P to go low and FSAT-N to go high. When FSHR-N goes high, FF3 is set activating G4 which activates G5. The next positive going edge out of I3 triggers state generator U34 causing FSRS-P to go high and FSBR-N to go low. The output of I2, FSBR-N, presets FF5 which disables G5. The second positive going edge out of I3, after FSHR-D: goes low, triggers state generator U34 causing FSBS-P to go low and FSBR-N to go high.

5-705. While FSBS-P is high and FSBR-N is low, **OFDN-N,** IFND-N, 1FW1-N, 2nd FW1S-P are generated. OFDN-N is generated when FSBR-N activates G38 which enables G39 to be activated by CF1A-P. G32 is enabled by FSBS-P and activated by CFOA-P which activates G33. **The** outputs of G39, OFDL-N, and G33, 1FND-N are routed to the Program: Maintenance Panel INFIBUS access circuit to gain access to the INFIBUS. FSBS-P enables G11, G15, G17 and G18. CF1A-P activates G15 which ensures FF8 is cleared. CFOA-P activates G11, G17, and G18. The output of G17 ensures FF10 is cleared. The output of G18 presets FF11 which remains preset until FSAS-P is generated again. FSPS-P enables G31 and FSPR-N disables G27. The output of G11, 1FW1-N, presets FF2 causing FW1S-P (waveform L, figure 108) to go high FHTR-N activates G57 which enables G51. G49 is enabled by FRNS-P. FRNR-N activates G58 which enables G59. When FW1S-P goes high, G49, G51, and G59 are activated causing RNDB-P and HTDB-P to go high and CRAB-N to go low. With ARAB-P and CRAB-N low, the CPU control register address is strobed to the INFIBUS address lines when INFIBUS access is gained. With RNDB-P and HTDB-P high and VADB-P low, the step command is strobed to the INFIBUS data lines when INFIBUS access is gained.

5-706. When the Program Maintenance INFIBUS access logic circuit receives DONE-N or QUIT-N from the CPU, FNDR-N or FATR-N goes low. FNDR-N or FATR-N activate G3 which activates G2. The next positive going edge out of I3, after FNDR-N or FATR-N goes low, triggers state generator U34 which causes FSCS-P to go high. FSCS-P activates G31 and G40. The output of G31 is inverted by I14 (OA1G-N). The output of G31 also triggers single shot SS1 which activates G33, causing 1FND-N to go low for 1.9 msec. The output of G40 is inverted by I15 causing OFW1-P to go high which clears FF2 and ensures FF1 is cleared. The output of G31 also enables G34 which is activated by CFOA-P. The output of G34, 1FW2-N (waveform O, figure 107), presets FF1. The output of G40 also activates G38 which enables G39 to be activated by CF1A-P. The output of G39, the second OFDN-N pulse, and 1FND-N are routed to the Program Maintenance Panel INFIBUS access circuit to gain access to the INFIBUS a second time. However, because FF2 has been cleared FW1S-P is low which disables G49, G51, G56, and G59. When G56 and G59 are disabled, ARAB-P is low and CRAB-N is high which causes the selected CPU register address to be strobed to the INFIBUS address lines when INFIBUS access is gained. With G49 and G51 enabled and G50 disabled (F1SS-P low) commands RNDB-P and HTDB-P are high, with VADB-P low. THis causes no information (zero address) to be strobed to the INFIBUS data lines when INFIBUS access is gained and the information from the selected CPU register address is displayed by the data LEDS.

5-707. When the QUIT-N pulse or second DONE-N pulse is received, FNDR-N or FATR-N goes low again, G3 is activated which activates G1. The next positive going edge out of I3, after FNDR-N or FATR-N goes low, triggers state generator U34, causing FSDS-P (waveform P, figure

107) to go high and FSDR-N to go low. FSDS-P activates G40 which activates G38, enabling G39. CFlA-P activates G39, generating the third OFDN-N pulse. The output of G40 is inverted by I15, generating the second OFWl-P pulse which resets FFl and FF2. FSDR-N activates G29, G42, and G46. The output of G46 goes low and is routed to the Program Maintenance Panel switch flip-flops and single action discriminator circuit. The output of G42 goes low which clears FF5. When DONE-N or QUIT-N was received FDNS-P went high, enabling G30. The output of G29 (high) also enables G30. CFIA-P activates G30 causing IFAD-N to go low which sets FF10. The output of FF10 is inverted by Ill which causes the done LED (CR57) to light. FF10 remains set until another master reset pulse, MRES-N, is received or until FSBS-P is generated again which will only occur with another switch closure on the Program Maintenance Panel switch flip-flops and single action discriminator circuit.. The next positive going edge out of I3 triggers state generator U34, causing FSDS-P to go Pow and FSDR-N to go high. Because state generator U34 is in its quiescent state (all outputs Pow) all operations in the Program Maintenance Panel state generation and micro operations circuit cease until OSTS-P is generated by another switch closure in the Program Maintenance Panel switch flip-flops and single action discriminator circuit, an address halt is required, or an address recognition occurs.

5-708. When the address write switch on the Program Maintenance Panel switch flip-flops and single action discriminator is touched, operation is the same as when the halt switch is touched, except FWRR-N goes low and FWRS-P goes high. When FWRR-N goes low, gates G53 and G54 are activated. The output of G54 activates gate G55. The output of G55 is inverted by inverter I23 which enables gate G56. The output of G53 enables gate G52. When FW1S-P goes high, G52 and G56 are activated causing DRDB-N to go low and ARAB-P to go high. With ARAB-P and CRAB-N high, the address determined by the address switches is strobed to the INFIBUS address lines when INFIBUS access is gained. With DRDB-N, RDNB-P, VADB-P, and HTDB-P low, the data determined by the data switches is strobed to the INFIBUS when INFIBUS access is gained. This action causes the data displayed to be written into the address displayed. FWRS-P is routed to gate G19 which is permanently disabled by inverter I12. FWRS-P also enables gate G26 which is activated by CFOA-P when FSAS-P is high. The output of G26 ensures FF12 is set and clears FF13. However, because G19 is disabled no further action occurs.

5-709. When the address read switch on the Program Maintenance Panel is touched, operation is similar to when the halt switch is touched, except FRDR-N goes low and FRDS-P goes high. When FRDR-N goes low G54 is activated which activates G55. The output of G55 is inverted by I23 which enables G56. When FWlS-P (waveform L, figure 108) goes high, G56 is activated causing ARAB-P to go high. With ARAB-P and CRAB-N high the address determined by the address switches is strobed to the INFIBUS address lines when INFIBUS access is gained. With RNDB-P, VADB-P, and HTDB-P low and DRDB-N high, no information (zero address) is strobed to the INFIBUS data lines when INFIBUS access IS gained and the device addressed (slave) places its data on the INFIBUS data lines. *This* data is displayed by the data 0 through 15 LEDS in the Program Maintenance Panel address/data switch identification, multiplexers, and LED circuit. G23 is enabled when FRDS-P goes high and activated by CFOA-P when FSAS-P goes high. The output of G23 ensures FF13 is set and clears FF12. The output of FF12 enables G22. If the address read switch is touched a second time, without touching any other switch that would set FF12 and FF13, FRDS-P goes high a second time activating G22. The output of G22 activates G20 which enables G21. G21 is activated by CFIA-P when FSAS-P is high. The output of G24, IFNC-N, causes the address shift register in the Program Maintenance Panel address/data switch identification, multiplexers, and LED circuit to increment by two before INFIBUS access is gained. This

second FRDS-P pulse also enables G23 which is activated a second time by CFOA-P when FSAS-P is high. The output of G23 now ensures FF12 is cleared and FF13 is set. The above action continues as long as only the address read switch is touched.

5-710. When the register write switch on the Program Maintenance Panel is touched, operation is similar to when the halt switch is touched, except FWGR-N goes low. When FWGR-N goes low G53 is activated which enables G52. FW1S-P activates G52 causing DRDB-N to go low. With ARAB-P low and CRAB-N high, the address determined by the register 0 through 15 switches is strobed to the INFIBUS address lines when INFIBUS access is gained. With RNDB-P, VADB.-P, HTDB-P, and DRDB-N low, the data determined by the data 0 through 15 switches is strobed to the INFIBUS data lines when INFIBUS access is gained.

5-711. When the resister read switch is touched, operation is similar to when the halt switch is touched, except all signals from the Program Maintenance Panel switch flip-flops and single action discriminator circuit are inactive and ANRW-N is generated. With these signals inactive, ARAB-P is low and CRAB-N is high which causes the address determined by the resister 0 through 15 switches to be strobed to the INFIBUS address lines when INFIBUS access is gained. Also, with these signals inactive RNDB-P, VADB-P, and HTDB-P are low and DRDB-P is high which prevents any data from being strobed to the INFIBUS data lines when INFIBUS access is gained and the addressed CPU register places its data on the INFIBUS data lines. This data is displayed by the data 0 through 15 LEDS.

5-712. When the address halt, adh, switch is touched, FAHS-P goes high and if the Program Maintenance Panel is not strobing information to the INFIBUS, STRE-P and STRD-P are low. When STRE-P and STRD-P are low, gate Gl2 is disabled and the high output of inverter I10 *and* FAHS-P enables gate G10. When the address on the infibus is the same as the address determined by the address switches, EOA4-P goes high and G10 is activated which presets FF7. The output of FF7 enables gate G14 which is activated by CFOA-P. The output of G14 presets FF9 which enables G13 and causes FCPR-N to go low. FCPR-N activates G4 and the output of G4 activates G5. The next positive going edge out of I3 triggers state generator U34 causing FSBS-P to go high and FSBR-N to go low. The output of I2, FSBR-N, presets FF5 which disables G5. The positive going edge out of I3, after FF5 is preset, triggers state generator U34 causing FSBS-P to go low and FSBR-N to go high. While FSBS-P is high and FSBR-N is low, OFDN-N, lFND-N, and FWlS-P are generated, as explained previously. Also while FSBS-P is high, G15 is activated by CFlA-P which clears FF8. G15 is then activated by CFOA-P which presets FF8. FF8 remains set until the next FSBS-P pulse is generated. When FACR-N goes low, G57 and G58 are activated. The output of G56 enables G51 (SARO-N high) and the output of G58 enables G59. When FWlS-P goes high G51 and G59 are activated causing HTDB-P to go high and CRAB-N to go low. Under these conditions the CPU control register address and halt command are strobed to the INFIBUS address and data lines, respectively, when INFIBUS access is gained.

5-713. When the Program Maintenance Panel INFIBUS access circuit receives DONE-N or QUIT-N from the CPU, FNDR-N or FATR-N goes low. FNDR-N or FATR-N activates G3 which activates G2. The next positive going edge out of I3, after FNDR-N or FATR-N goes low, triggers the state generator U34 which causes FSCS-P to go high. FACS-P is enabling gate G37 and FACR-N is disabling gates G28, G36, and G44. FSCS-P activates G27 and G40. The output of G40 is inverted by I17 causing OFWl-P to go high which clears FF2 and ensures FF1 is cleared. The output of FF1 now disables G2 and the next positive going edge out of I3 causes FSCS-P to go low. The output of G40 also activates G38 which enables G39 to, be activated by CF-lA-P. The output of G39, the second OFDN-N pulse is routed to the Program Maintenance Panel

INFIBUS access circuit. The output of G27 is routed to G28 which is disabled by FACR-N. CFOA-P activates G37 causing OFCP-P to clear FF7 and FF9. Because state generator U34 is now in its quiescent state (all outputs low), all operations in the Program Maintenance Panel state generation and micro operations circuit cease until the run or step switch is touched.

5-714. When the attention, attn, switch on the Program Maintenance Panel miscellaneous control circuit is touched the Program Maintenance Panel INFIBUS access circuit generates a level 1 interrupt. In addition, the Program Maintenance Panel state generation and micro operations circuit causes the Program Maintenance Panel address, FF80 16, to be strobed to the INFIBUS data lines when INFIBUS access is gained. When the attn switch is touched, FlSS-P goes high and, if an address recognition has not occurred (SARO-N high), G50 is activated causing VADB-P to go high. With RNDB-P and HTDB-P low and VADB-P high, the Program Maintenance Panel address is strobed to the INFIBUS data lines when INFIBUS access is gained.

5-715. When the Program Maintenance Panel is operating in the slave mode, SARO-N goes low when the Program Maintenance Panel address multiplexer, bus driver receiver and recognition circuit detects the Program Maintenance Panel address on the INFIBUS address lines. SARO-N disables G49, G50, and G51 which causes RNDB-P, VADB-P and HTDB-P to remain Pow. SARO-N is also Inverted by inverter I22 which enables G52. The output of I22, SARP-P, is routed to the Program Maintenance Panel INFIBUS access circuit to enable either the information determined by the address switches or by the data switches to be strobed to the INFIBUS data lines. If AOIA-P is low, DRDB-N is high and the information determined by the address switches is strobed to the INFIBUS data lines. If AOIA-P is high, G52 as activated and DRDB-N is low, and the information determined by the data switches is strobed to to the INFIBUS data lines.

5-716. PROGRAM MAINTENANCE PANEL INFIBUS ACCESS LOGIC CIRCUIT.

5-717. General. The Program Maintenance Panel INFIBUS access circuit detects when the Program Maintenance Panel state generation and micro operations circuit is requesting an INFIBUS access for a direct data transfer and causes the direct data transfer to occur. These circuits also detect when the state generation and micro operations circuit is requesting a level 1 interrupt to be generated and generates the level 1 interrupt. If the function addressing the Program Maintenance Panel is writing into the Program Maintenance Panel, the Program Maintenance Panel INFIBUS access logic circuit also causes the information on the INFIBUS data lines to be displayed by the address or data LEDS. If the function addressing the Program Maintenance Panel is reading from the Program Maintenance Panel, the information from the address shift register or data shift register is strobed to the INFIBUS data lines.

5-718. Detail Analysis (see figure 108). When the Program Maintenance Panel state generation and micro operations circuit receives a master reset pulse, MRES-N, MREU-N goes low for the duration of MRES-N. MREU-N clears flip-flops FF3, FF6, FF9, FF10, FF12, and FF14, activates gate G15 which resets flip-flop FF4, activates gate G18 which resets flip-flop FF5, and activates gates G16 and G35. The output of G35 is inverted by inverter I14 which clears flip-flop FF13. The output of G16, RFlS-N, activates gate G25 which clears flip-flop FF8. With FF6 and FF8 cleared, gate G24 is activated which clears flip-flop FF11.

5-719. When the Program Maintenance Panel INFIBUS access circuit is required to gain INFIBUS access and perform a direct data transfer, 0FND-N (waveform A, figure 109) and 1FND-N (waveform B, figure 109) are generated by the Program Maintenance Panel state generation and micro operations circuit. 0FND-N ensures FF9, FF10, and FF14 are cleared. The trailing edge of 1FND-N presets FF5,

causing FNDS-P (waveform C, figure 109) to activate gate G19. The output of Gl9 sets FF6. The 0 **output** of FF6 disables **gates** G14, G21, and G31 and activates gate G25 which ensures FF8 is cleared. If no other function is generating SELD-N, gate G29 is enabled and the 1 output of FF6 activates G29. The output of G29 sets FF11 which activates gate G20. The **output** of G20 presets flip-flop FF7, if it is not already preset by a previous direct data transfer, and is coupled through driver DR3 causing SRLD-N (waveform D, figure 109) to go low. Presetting FF7 disables gate G14 and enables gates G17, G23, and G26. In response to SRLD-N the Bus Controller causes SELD-N (waveform E, figure 109) to go low and generates the precedance pulse PCDA-P. When SELD-N goes low, G29 is disabled, FF12 remains set, gate G30 is activated, and gate G33 is enabled. The low output of G30 disables gate G28. When the precedance pulse, PCDA-P (waveform F, figure 109), is received, G33 is activated. The output of G33 sets FF13 and disables gate G34. The 0 output of FF13 disables gates G20, G22, G27, G.29, and G38 and. is coupled through driver DR5 causing SACK-N (waveform G, figure 109) to go low. The 1 output of FF13 enabies G34 and activates gate G37 which sets FF12. The 1 output of FF12 is routed to gates G26, G27, G36, and G38. The 0 output of FF12, FOLR-N, disables G19, G21, and G29. The 0 output of FF12 is also coupled through inverter I3 causing AOUT-P to go high and it also activates gate G3 causing DOUT-P to go high. AOUT-P strobes the address to the INFIBUS address lines and DOUT-P strobes the data to the INFIBUS data lines. AOUT-P also activates gate G1 because FMRS-P is low except for address read, resister read, or step switch closures. When an address read switch closure is detected, FRDS-P and SBCP-P go high which activates gate G11. The output of G11 sets FF3. The output of G13 activates gate **G12** causing DSCB-N to go low and is inverted by inverter I9 causing FMRA-N to go low. The output of FF3, FMRS-P, also disables G1 preventing RITE-N from going low during an address read operation. When a resister read switch closure is detected, FRGS-P and SBCP-P go high which also activates G11, and DSCB-N, FMRA-N, and FMRS-P are generated as explained. When a step switch closure is detected, OAlG-N goes low when the second INFIBUS access is requested (reading data from selected CPU register). OAlG-N sets FF3 and DSCB-N, FMRA-N, and FMRS-P are generated as explained. The 0 output of FF12 is also inverted by inverter I13. The output of I13 enables gate G32 and delay DL2 causes G32 to be activated 50 nsec after it is enabled. The output of G32, STRF-N is coupled through driver DR2 causing STRB-N (waveform H, figure 109) to go low. Before STRB-N is generated PCDA-P returns to low which disables G33. This high output of G33 activates G34 which clears FF11. Clearing FF11 disables G20 which causes SRLD-N to go high. The output of DR2, STRB-N, is also coupled through inverter I4 which activates gate G37. The output of G37 clears FF13 enabling G27, G29, and G38, disabling G34 and G37, and causing SACK-N to go high.

5-720. When the direct data transfer is completed the addressed function receiving the data generates DONE-N. DONE-N is inverted by inverter I6 causing DONF-P to go high which activates G27. The output of G27, DONP-N, clears FF6 and is inverted by inverter I12. The output of I12 activates gate G23 which presets FF9. FF9 remains set until the next OFDN-N pulse is received. DONP-N also activates gate G13. The output of G13 is inverted by inverter I10 which clears FF3 and disables G12. The output of G13 also activates G17. The output of G17 activates G18 which resets FF5 causing FNDS-P to go low which disables G19. Clearing FF6 activates G24 and enables gate G31. The output of G24 ensures FF11 is cleared. When DONE-N returns to high-, DONF-P goes low and the output of G27 goes high activating G31 which clears FF12. The 0 output of FF12 is coupled through I13 which disables G32 causing STRB-N to go high. Clearing FF12 also disables G26, G27, G36 and G38.

5-721. If DONE-N is not generated within 2 usec after STRB-N is generated, the Bus Controller generates QUIT-N. QUIT-N is inverted by inverters I16 and I17. The output of I17 disables G37. The output of I16 activates G26 (FF11 still set). The output of G26 presets FF10 causing FATR-N to go low. The output of I16 also activates G38 which sets FF14. The output of FF14 clears FF12 which disables G26. FF10 remains set until the next OFDN-N pulse is received.

5-722, When the attn switch on the Program Maintenance Panel miscellaneous control circuit is touched, the Program Maintenance Panel INFIBUS access circuit causes a level 1 interrupt to be generated. 1.9 msec after the attn switch is touched FTTR-N goes low and remains low for 24 msec after the attn switch is released. After the release of the attn switch, OFDN-N goes low which clears FF9, FF10, and/or FF14, as necessary. For the following discussion assume all flip-flops are initially reset either by the completion of a direct data transfer, the generation of a previous level 1 interrupt, or receipt of a master reset pulse, MRES-N. FF4 sets on the trailing edge of FTTR-N. The output of FF4 is inverted by inverter I11, causing FNlL-N to go low which causes the attn LED (CR66) to light. The output of FF4 also disables G15 causing RFl5-N to go high. RFlS-N being high disables G25 and FNlS-P activates gate G21 which sets FF8. The 0 output of FF8 disables G19, G24, and G31. The 1 output of FF8, FlSS-P, enables G22 and activates G29 if no other function is generating SELl-N. If another function is generating SELl-N when SELl-N goes high, G29 is activated. The output of G29 now sets FF11 and disables G30 and G33. The output of FF11 enables G30 and G33 and activates G22. The output of G22 resets FF7, if it was preset, and is coupled through driver DR4 which generates SRLl-N. Resetting FF7 enables G14 and disables G17, G23, and G26. In response to SRLl-N the Bus Controller causes SELl-N to go low and generates the precedence pulse PCDA-P. When SELl-N goes low, G29 is disabled, FF11 remains set, G30 is activated and G33 is enabled. The output of G30 disables G28. When the precedence pulse, PCDA-P, is received G33 is activated which sets FF13 and disables G34. The 0 output of FF13 disables G20, G22, G27, G29, and G38 and is coupled through DR5 causing SACK-N to go low. The 1 output of FF13 enables G34 and activates G37 which' sets FF12. The 1 output of FF11 is routed to G26, G27, G36, and G38. The 0 output of FF12, FOLR-N, disables G19, G21, and G29. The 0 output of FF12, is also coupled through I3 causing AOUT-P to go high and it also activates G3 causing DOUT-P to go high. AOUT-P now causes the Program Maintenance Panel address to be strobed to the INFIBUS address lines and DOUT-P causes no data (zero address) to be strobed to the INFIBUS data lines. Because G11 is not activated, FF3 is not set and FMRS-P remains high which enables G1 causing RITE-N to go low when AOUT-P goes high. RITE-N is also inverted by inverter I1 which enables gate G6. The 0 output of FF12 also generates STRB-N, as explained previously. Before STRB-N is generated PCDA-P returns to low which disables G33. This high output of G33 activates G34 which clears FF11. Clearing FF11 disables G22 which causes SELl-N to go high. The output of DR2, STRB-N, is also coupled through I4 activating G37. The output of G36 clears FF13 which enables G27, G29, and G38 and disables G34 and G37, When STRB-N goes low, the address recognition signal SARP-P from the Program Maintenance Panel state generation and micro operations circuit goes high which activates G6. When the attn switch is touched OLTS-P goes high which disables gate G7. Theoutput of G6 activates gate G4 which triggers single shot SSl. The output of SSl returns to high 100 nsec after it is triggered which presets flip-flop FF2. Gate G8 is disabled by G7. The output of FF2 activates gate G5. The output of G5 is coupled through DRl which generates DONE-N. The output of FF2 is also inverted by inverter I5. The output of I5 is delayed 50 nsec by delay DL2. After this 50 nsec delay, G5 is disabled which causes DONE-N to go high. DONE-N is also inverted by I6 causing DONF-P to go high which activates G27 clearing FF8. DONP-N also activates G13. The output of G13 is

inverted by I10 which ensures FF3 is cleared. The output of G13 also activates G14 which activates G16. The output of G16 resets FF8. The output of FF8 is inverted by I11 causing the ATTN LED to go out. RElS-N activates G25 which ensures FF8 is cleared. With FF6 and FF8 cleared, G31 is enabled. When DONE-N returns to high, G27 is disabled. This high output of G27 activates G31 which clears FF12. The 0 output of FF12 IS inverted by I13 which disables G32. The output of I13, STRF-N, is also coupled through DR2 causing STRB-N to return to high. When STRB-N goes high, the output of I4 resets FF2, ensures FF1 is cleared, and SS1 is reset.

5-723. If DONE-N is not generated within 2 usec after STRB-N goes low, the Bus Controller generates QUIT-N. QUIT-N is inverted by I16 and I17. The output of I17 disables G37. The output of I16 activates G38 which sets FF14. The output of FF14 clears FF12 causing STRB-N to go high and FFl, FF2, and SS1 are reset, is explained previously.

5-724. If RITE-N is low (another function writing into the Program Maintenance Panel) the output of I2 enables G6. When the Program Maintenance Panel recognizes its address on the INFIBUS address lines (slave, mode), SARP-P goes high activating G6. The output of I2, is also coupled through I3 which disables G2. The output of G6 activates G4 and G7 because OLTS-P is low. The output of G4 triggers SS1 **which disables** gate G8 for 100 nsec and presets FF2. When the output of SS1 returns to high, G8 is activated causing SWRG-P **to go high.** If ABOl-N is low, G10 is enabled inverter I7 and G9 is disabled by inverter I8 SWRG-P activates G10 causing DSCB-N to go low and the information **on the INFIBUS data lines is displayed by the** data LEDS. If AB01-N is high, G9 is enabled by I7 and G10 is disabled by I7. SWRG-P now activates **causing ASCB-N to go low and** the information on the INFIBUS data lines is displayed by the address LEDS.

5-725. If RITE-N is high (another function reading from Program Maintenance Panel), the output of I2 disables G6 and is coupled through I3 enabling G2. When the Program Maintenance Panel recognizes its address on the INFIBUS address lines (slave mode), SARP-P goes high activating G2. The output of G2 sets FFl. The output of FF1 activates G3 causing DOUT-P to go high. If ABOl-N is low, AOIA-P is high, and DOUT-P strobes the information stored in the data shift register of the Program Maintenance Panel address/data switch identification, multiplexers, and LED circuit to the INFIBUS data lines. If ABOl-N is high, AOIA-P is low and DOUT-P strobes the information stored in the address shift register of the Program Maintenance Panel address/data switch identification, multiplexers and LED circuit to the INFIBUS data lines. The output of FFl also activates G4 which triggers SSl. The trailing edge of the 100 nsec pulse out of SSl presets FF2 which activates G.5. 50 nsec later G5 is disabled by I5 and DLl. This low output of DL2 resets FFl which causes DOW-P to return to high by disabling G3. This SO nsec pulse out of G5 is coupled through DRl causing DONE-N to go low for 50 nsec. At the end of the DONE-N pulse the module addressing the Program Maintenance Panel causes STRB-N to go high and removes the Program Maintenance Panel address from the infibus address lines which causes SARP-P to go low. When SARP-P goes low G2 is disabled and STRB-N via I4 clears FF1.

5-726. CORE MEMORY DETAIL LOGIC DIAGRAM DESCRIPTION.

5-727. The following paragraphs contain the detail logic diagram descriptions of the Core Memory. The Core Memory is divided into three main circuit areas as follows: the timing and control logic circuit; address register, decoding, switching, and control and buffer logic circuit; and sense, inhibit, and data circuit.

5-728. TIMING AND CONTROL LOGIC CIRCUIT.

5-729. General. The timing and control logic circuit is controlled by the Processor Core Memory Controller. This circuit determines whether the Core Memory will operate in the clear/write or read restore mode.

5-730. Detail Analysis (See figure 110). At turn-on, PWR RDY-P enables gate G3. After the 4 usec delay of delay DLl, G3 is activated which turns off transistor switch Ql, causing GEN RST-N to go high. While GEN RST-N is low (before G3 is activated), flip-flop FF1 is cleared and gate G20 is activated. The 1 output of FFl, BUSY-N (low), presets flip-flops FF5 through FF7 and FF10 and FF11. At this time, BUSY-N also activates gate G2 which generates BUSG-N. BUSG-N presets flip-flops FF8, FF9, and FF12. GEN RST-N also activates gate G14 which presets flip-flop FF2, resets flip-flop FF3, and generates CYC END-N. If PWR RDY-P goes low (power failure has occurred) and BUSY-N is low, the output of G1 goes high causing GEN RST-N to go low. However, if PWR RDY-P goes low during a memory cycle (BUSY-N high) the output of G3 rernains low until BUSY-N goes low which disables G3. Disabling G3 turns on transistor switch Ql which generates GCN RST-N, Another memory cycle cannot be started until PWR RDY-P returns to logic 1.

5-731. In the clear/write mode RD INIT-P and RD ONLY-P are logic 0 and FULL CYC-P and MEM SEL-P are logic 1. Under these conditions, WT INIT-P (waveform A, figure 111) activates gate G7 which sets FFl. The output of G7 activates gate G11 which generates AIX-P (waveform B, figure 111). The output of G7 also clears flip-flop FF4. AM-P clocks the address register decoding, switching, and control and buffer logic circuit. Disabling G8 activates gate G5 which enables the ossscillator consisting of gates G5 and G6 and the phase shifter. The output of G5 is inverted by inverter I1 which generates CLOCK1-P (waveform C, figure 111). The output of G6 is inverted by inverter I2 which generates CLOCK2-P (waveform D, figure 111). CLOCKl-P and CLOCK2-P trigger FF5 through FF12.

5-732. The output of G7, CWST-N (waveform S, figure 111), activates gate G34 generating PRE YRT-P (waveform T, figure 111) which is routed to the address register, decoding, switching, and control and buffer logic circuit. The output of G34 is inverted by inverter I5 which causes gate G23 to go to logic 1 enabling gates G1, G28, G31, G32, G35, G36, and G37 and single shot SS2. Gate G30 generates a 200 nsec positive pulse that activates G31. The output of G31, MRT-N (waveform U, figure 111), is applied to the address register, decoding, switching, and control and buffer logic circuit to allow current flow in the core stack, thereby clearing the cores. The logic 0 output of I5 is inverted by inverter I6 which activates G35. The output of G35, RDR-P (waveform V, figure 111), resets the data registers in the sense, inhibit, and data circuit. G28 generates a 60 nsec negative pulse that activates gate G29. G29 generates DIX-P (waveform W, figure 111) that clocks the data into the sense, inhibit, and data circuit data registers. When the output of G21 returns to logic 1, gate G26 is activated because RD ST-N (waveform X, figure 111) and CW ST-N are logic 1. Gate G27 generates a pulse whose leading edge is determined. by T40-P and trailing edge by T120-P. The output of G27 is inverted by invertcr I4 and routed to the Core Memory sense, inhibit, and data circuit as TINH-P (waveform Y, figure 111) generating the inhibit current through the cores where a zero is to be stored. TINH-P is also inverted by invcrter I3 and **pulse** shaper C23, R35, and R36 generates a 33 nsec positive pulse on the trailing edge of TINH-P which activates gate G13. The output of G13 activates G14 **which gener**ates CYC END-N. CYC END-N is applied to the Core Memory address register, de**coding, switching, and control a n d b u f f e r** logic circuit to set the cycle busy flip-flops. FF12 and FF13 are not affected because FF2 is set and FF3 is reset. Gate G22 is enabled when cross-coupled

gates G20 and G23 are reset at 320 nsec. The leading edge **of** MWT-P **(waveform 2,** figure 111) is determined by T200-P **and** trailing edge by T260-P. MWT-P is **ap**-plied to the address register, decoding, switching, and control and buffer logic circuit, resulting in the generation of X and Y write currents.

5-733. CLOCKl-P triggers FF5 through FF8 and CLOCK2-P triggers FF9 through FF12. At the start of each cycle the 0 outputs of FFS through FF12 are logic 0 **(pre**-set). The first CLOCKl-P pulse clears FF5, the second CLOCKl-P pulse clears FF6 and so on until FFS through FF8 are cleared. The 0 output of FF8 is now logic 1 and the continuing clock pulses set FF5 through FF8. FF9 through FF12 operate in the same manner as FFS through FF8.
FF5 through FF12 produce a series of timing pulses at 20 nsec intervals (waveforms E through Q, figure 111).

5-734. When FFl sets, the 0 output activates gates G15 and G16. The output of G16 activates gate G17 causes MEM AVAIL-P (waveform R, figure 111) to go to logic 0, informing the Processor that the Core Memory is not available. The output of G15 is delayed 50 nsec by delay DL2 which activates gate G10 disabling gates G4, G7, and G8. At 550 nsec, single shot SSl is triggered by T260-P and T340-P causing its output to go to logic 0 for 200 nsec. At 600 nsec, gate G9 is activated by T300-P and T180-P which clears FFl and disables the oscillator (G6). Clearing FFl presets FF5 through FF12. The output of SSl holds MEM AVAIL-P at logic 0 and disables G4 and G7 via' G15, DL2 and G10 until the output of SSl returns to logic 0.

5-735. Gates G36, G37, and G38 and delays DLS and DL6 generate MSAS-P (waveform AA, figure 111) whose leading edge is determined by T200-P and trailing edge by T80-P.

5-736. In the read/restore mode WT INIT-P and RD ONLY-P are logic 0 and FULL CYC-P and MEM SEL-P are logic 1, under these conditions **RD INIT-P (waveform AB, figure 111) is gated through G4 to set FFl arid FF4. Operation is similar to the clear/** write mode except setting FF4. enables single shot SS2. SS2 generates a 100 nsec pulse when **RD PHS-P (waveform AC,** figure 111), T260-P, and T140-P are logic 1. The **output of SS2 activates gate G18** which generates DATA AVAIL-N (waveform AD, **figure 111) notifying the Processor** that data is available. The logic 1 output of FF10, RR-P/CW-N, also enables the sense, inhibit, and data circuit. MSAS-P now causes the **data** to be strobed out of the Core Stack (read mode) and into the data registers of the sense, inhibit, and data circuit. TINH-P and MWT-P cause this data to be restored into the cores.

5-737. ADDRESS REGISTER, DECODING, SWITCHING, AND CONTROL AND BUFFER LOGIC CIRCUIT.

5-738. General. The address register, decoding, switching, and control and buffer logic circuit stores address bits 00 through 15. Address bits 00 through 06 are X address bits and address bits 07 through 12 are Y address bits. Address bits 00 through 12 select the CM BSM core memory stack address where the data is to be stored. Address bits 13, 14, and 15 are decoded to produce the various BSM select signals.

5-739. Detail Analysis (See figure 112). The address register functions as an open latch for address bits AIOO-P through AIOS-P and AI07-P through AI12-P. Flip-flop FFl is reset at the end of a memory cycle by CYC END-N. If AIOO-P goes high when FF1 is reset the output of gate G1 goes low which is inverted by inverter I1, causing MAROO-P to go high. 40 nsec later T200-P goes low presetting FFl which causes the high output **of** inverter I1 and the 1 output of FFl to hold the output of Gl low. The 1 output of FFl prevents any changes in AIOO-P from effecting G1. At the end of a memory cycle CYC END-N goes to logic 0 for 33 nsec resetting FFl which enables G1 again. AIO6-P is clocked into flip-flop FF2 on the leading edge of AIX-P (waveform A, figure 113)

setting FF2. The 0 output of FF2 is inverted by inverter I2 which generates MAR06-P. AI13-P, AI14-P, and EI15-P are inverted by inverters I3, I5, and I7. The outputs of I3, I5, and I7 are clocked into FF3, FF4, and FF5 on the leading edge of AM-P. The outputs of FF3, FF4, and FF5 are applied to the BSM select decoder U39, U40, and U41 which generates the required BSM select signal, BSM00-P through BSMO4-P, to enable the selected CM BSM. The following discussion assumes that the first BSM is being selected (BSMOO-P high).

5-740. During a read cycle, PRE YRT-P (waveform B, figure 113) activates gate G2 which determines the leading edge of YRT-N (waveform D, figure 113). MRT-N (waveform C, figure 113) is inverted by inverter I6 which determines the trailing edge of YRT-N. The output of I6 also activates gate G3 which generates XRTl-P. The output of G3 also activates gate G4. Address decoder U17 is enabled by the output of G4 and decodes MAROO-P through MAR02-P causing one of the address decoder output lines to go low. This low level is applied to the pulse transformer which causes the transistor switch to generate a positive pulse on the selected line, XCAOO-P through XCAO7-P. XRTl-P enables G8 and G9 and if MARO6-P is high the output of driver DR2, MA 06-P, is high, G9 is activated which enables address decoder U23. If MAR06-P is low the output of inverter I4 is high, G8 is activated which enables address decoder U19. Address decoders U19 and U23 decode MARO3-P through MAR0 5-P and cause one of 16 outputs to go low. This low level is applied to the pulse transformer which causes the transistor switch to generate a negative pulse on the selected line, XSOO-P through XS15-P. The XS line selects one group of 8 Pines out of 16 groups and the XCA line selects one line of the group of 8 and allows X read current to flow through the selected X core lime from the XS line to the XCA line. The X core line is threaded through 18 cores, owe in each mat (each mat has 8192 cores). YRT-N enables address decoders UI8 and U2I. Address decoder Ul8 decodes MAR0 7-P through MAR09-P causing one of the output lines to go low. This low level is applied to the pulse transformer which causes the transistor switch to generate a positive pulse on the selected line, YCAOO-P through YCAO7-P. Address decoder U21 decodes MAR10-P through MAR12-P causing one of the output lines to go low. This low level is applied to the pulse transformer which causes the transistor switch to generate a negative pulse on the selected line, YSOO-P through YSO7-P. The YS line selects a group of 8 lines out of 8 groups and the YCA line selects one line of the group of 8 and allows Y read current to flow through the selected Y core line from the YS line to the YCA line. The Y core line is threaded through 18 cores, one in each mat. When X and Y read current flows through the selected core and if the core is in a 1 state, the core turns over (returns to 0 state) generating a pulse on the sense/inhibit line.

5-741. During a write cycle, MWT-P activates gate G5 which generates WTl-P (waveform E, figure 113). WTl-P is inverted by inverter I8 which enables address decoder U13. Address decoder U13 **decodes** MAR00-P through MAR02-P causing one of the address decoder U13 output lines to go low. This low level is applied to the pulse transformer which causes the transistor switch to generate a negative pulse on the selected Sine, XCC00-N through XCCO7-N. WTl-P enables G6 and G7 and if MAR06-P is high the output of DR2 is high, G6 is activated which enables address decoder U24. If MAR06-P is low the output of J4 is high, which activates G7 enabling address decoder U15. Address decoders U15 and U24 decode MARO3-P through MAR05-P and cause one of 16 outputs to go low. This low level is applied to the pulse transformer which causes the transistor switch to generate a positive pulse on the selected line, XSOO-P through XS15-P. The XS line selects a group of 8 Pines out of 16 groups and the XCC line selects one line of the group of 8 and allows X write current to flow through the selected X core line from the XCC line to the XS line. WT2-N also enables

address decoders U14 and U16. Address decoder U14 decodes MAR07-P through MAR09-P causing one of the output lines to go low. This low level is applied to the pulse transformer which causes the transistor switch to generate a negative pulse on the selected line, YCC00-N through YCC07-N. Address decoder U16 decodes MAR10-P through MAR12-P causing one of the output lines to go low. This low level is applied to the pulse transformer which causes the transistor switch to generate a positive pulse on the selected line, YSOO-P through YSO7-P. The YS line selects a group of 8 lines out of 8 groups and the YCC line selects one line of the group of 8 and allows Y write current to flow through the selected Y core line from the YCC line to the YS line. When X and Y write current flows through the selected core a 1 is stored into the core if the sense/inhibit line does not have inhibit current flowing.

5-742. SENSE, INHIBIT, AND DATA CIRCUIT.

5-743. General. The sense, inhibit, and data circuit detects the low level output from the cores during a read cycle and converts this output to a high level signal which is gated into the data register. The data register stores this information until it is routed to the Processor and/or reshred into core. The data register also stores incoming data from the Processor during a write cycle. This incoming data is gated into the data register and the inhibit drivers generate inhibit current for all dates bits that are logic 0. Inhibit current, when present, runs parallel to and in the opposite direction from the Y write current, preventing the coincident X and Y write currents from switching the cores involved. In this way, data is restored into the core during rhe read/restore operation, and new data is stored during a clear/write operation.

5-744. Detail Analysis (see figure 115). MSAS-P (waveform A, figure 116) enables gates G1, G4, G5, and G6 which are activated by the BSM select signal, BSM00-P through BSM04-P. The BSM select signal generated determines which CM BSM will be enabled. The following discussion assumes that CM BSM 1 (BSMOO-P generated) will be enabled. The SASOO-P output of G1 activates gate G2 which is also enabled by BSMOO-P.

5-745. A single sense/inhibit line threads through all the cores corresponding to one data bit. The sense circuitry for each data bit is identical, therefore the following discussion discusses only the operation of the 00 bit. During a read cycle, the coincident X and Y currents cause the turn-over of a single core if a 1 has been stored. This turn-over induces a pulse of approximately 30mv across the S-00 input lines. This pulse is shaped by the pulse shaper CRl, CR2, and U2 and coupled through the impedance matching network Ul to the input of the differential line receiver U3. The differential line receiver U3 converts the low level output of the core (S-00) to digital levels (0 and 5 volts). The pulse output of the differential line receiver activates G3.

5-746. During a read cycle, RR-P/CW-N (waveform A, figure 115) activates gate G7 and is coupled through inverter I2. During a read cycle, ZW1-P and ZW2-P are logic 0 which activate gates G9 and G17 respectively. The output of G9 enables gates G11, Gl2, and Gl3 and the output of G17 enables gates G18, G19, and G20 The output of G7 is coupled through driver DRl which activates G12 and G19 generating DOXl-P and DOX2-P, respectively. RDR-P (waveform B, figure 115) activates G11 and G18 which generate RDR1-N and RDR2-N, respectively. MSAS-P (waveform C, figure 115) activates G13 and G20 which generates SAS1-P and SAS2-P, respectively. SAS1-P and SAS2-P are coupled through drivers DR2 and DR3 which enable the sense gates (G14 and G21 shown). The sense gates couple SAOO-P through SA17-P to the data register as MDROO-N through MDR17-N. Data registers 0C through 08 and 09 through 17 operate in exactly the same manner; therefore, the following discussion will discuss the operation of data register 00 through 08. When RDRl-N goes low, DIR1-N is

high and DIXl-P is low, causing the output of gate G24 to go high. At this time DOXl-P is high and the output of G24 activates gate G22 which causes DOOO-P to go low. The high output of G24 is applied to gate G25 which, with DIRl-N high, causes the output of G25 to go low. The low output of G25 is applied to G24 to hold the output of G24 high. The low output of G25 is also inverted by inverter I5 which causes DATA INHOO-P to go high. After the data register is reset, RDRl-P **returns to high** which enables G24. If a 0 is read from the core (SAOO-P low), MDROO-N is high and the data register does not change state. If a 1 is read from core, MDROO-N is low which is applied to the output of G24 and the input of G25 which changes the state of the data register. When MDROO-N goes low, G22 is disabled, which causes DOOO-P to go high. MDROO-N also disables G25 which activates G24 which holds G22 disabled. The high output of G25 is inverted by I5 which causes DATA INHOO-P to go low.

5-747. During a restore cycle TINH-P (waveform D, figure 115) is generated by the timing and control logic circuit, activating gate G29 which is enabled by BSMOO-P. The output of G29 is inverted by inverters I8, I9, and I10 which strobe the data inhibit drivers. SPWR-P activates gate G30 turning on transistor switches Q2 and Q3 which generate SVSl-P and 5VS2-P. 5VSl-P and 5VS2-P allow inhibit current to flow through the sense/inhibit lines of the core stack. If the data to be restored is logic 1 (DATA INHOO-P is logic 0), G28 is disabled and driver U13, 1Q1, does not generate inhibit current, INHOO-N. This causes the coincident X and Y current to store a 1 at the address location. If a 0 is to be restored (DATA INHOO-P is logic 1) **G28** is enabled and strobed by TINHl-P causing the output of G28 to go low. When the output of G28 goes low, driver U13, 1Q1, generates inhibit current; INHOO-N, which is driven through the sense/inhibit line, C-00, in the opposite direction from the current in the Y line. This causes the Y current to be algebraically neutralized and the core remains in the zero state.

5-748. During a write cycle, RR-P/CW-N is logic 0 and ZWl-P and ZW2-P are logic 1. RR-P/CW-N is inverted by I2 which activates G8 and G15. The output of G8 enables G10 and the output of G15 enables G16. DIX-P (waveform E, figure 115), from the timing and control logic circuits, activates GlO and G16 causing DIRl-N and DIR2-N to go to logic 0. DIRl-N is inverted by inverter I1 and DIR20N is inverted by inverter I3 causing DIKl-P and DIX2-P to go to logic 1. DIOO-P IS inverted by inverter I4. When DIOO-P is high, the output of I4 is low which disables G25. The high output of G25 is inverted by I5 which causes DATA INHOO-P to go low. DATA INHOO-P low prevents inhibit current, INHOO-N, from being generated, allowing a 1 to be stored in core as explained previously. If DIOO-P is low, the output of I4 activates G25 (DIXl-P logic 1). This low output of G25 is inverted by I5 causing DATA INHOO-P to go high which generates inhibit current, INHOO-Ni **causing** a 0 to be stored in core, as explained previously.

SECTION II

FUNCTIONAL OPERATION OF ELECTRONIC CIRCUITS

5-749. GENERAL.

5-750. This section contains information pertaining to the different types of printed circuit, (PC), cards used in the Processor and Core Memory. These include: 16 different types of PC cards used in the Processor, AlA3, and five different types used in the Core Memory, AlA8. The PC card information provided is of a general nature; detailed functional operation being provided in Section I of the chapter in the applicable detailed logic diagram descriptions.

5-751. Also included in this section are descriptions of " unique" integrated circuit, (IC), components. Unique IC's are defined as those IC's for which no internal logic is shown on the schematic diagrams in T.O. 3185-4-308-3, and the IC is being represented as a block with a functional name and reference designation. The IC descriptions provide a brief functional analysis of the logic contained in these components and, where required, a truth table is provided to simplify the discussion. For principles of operation of basic standard circuits, refer to T.O. 31-1-141.

5-752. PC CARD DESCRIPTIONS.

5-753. BUS CONTROLLER (8033 1160-000) (see figure 116). The Bus Controller (AlA3A5) contains two unique types of IC's (type SN74175N and P3404). The applicable paragraph describing these unique IC's are listed in table 5.-l. The Bus Controller primarily controls - all communications occurring on the INFIBUS, resolving priority of INFIBUS access requests. Other functions of the Bus Controller are alarm interrupt, master reset, and INFIBUS line loads. The alarm interrupt functions after a power line recovery is detected and either a level 4 interrupt service request or an autoload signal is initiated. The master reset signal is applied to the INFIBUS to initiate a master reset cycle immediately after power is applied or when the Program Maintenance Panel reset switch is touched. INFIBUS line loads are resistors on the Bus Controller which terminate all data, control, address, and status lines on the INFIBUS.

Table 5-1.

Integrated Circuit Descriptions

INTEGRATED CIRCUIT TYPE	PARA NO.	INTEGRATED CIRCUIT TYPE	PARA NO.	INTEGRATED CIRCUIT TYPE	PARA NO.
HD-0165	5-775	SN74100	5-786	SN74174N	5-797
N8202N	5-776	SN74138N	5-787	SN74175N	5-798
N8203N	5-777	SN74145	5-788	SN74178	5-799
N8235N	5-778	SN74150P	5-789	SN74181	5-800
N8264N	5-779	SN74151AJ	5-790	SN74182N	5-801
N8266B	5-780	SN74153N	5-791	SN74191	5-802
P3205	5-781	SN74154N	5-792	SN74197N	5-803
P3404	5-782	SN74157N	5-793	SN74198N	5-804
SN7442N	5-783	SN74161J	5-794	SN75453	5-805
SN7493A	5-784	SN74163N	5-795	U7B961459X	5-806
SN7496	5-785	SN74170N	5-796	U78961559X	5-807

5-754. CPB (80331220-000) (see figure 117). The CPB (AlA3A6) contains nine unique types or IC's (type SN7415OP, SN7415lAJ, SN74153N, SN74163N, SN74174N, SN74175N, P3205, N8264N, and N8235N). The applicable paragraph describing these unique IC's are listed in table 5-1. The CPB, in conjunction with a matched CPA, form the CPU which is used to process data that is received from either the Core Memory or other Processor modules under control of stored software programs. The CPB contains microcode control circuits of the CPU. The microcode control circuit consists of three registers (E, S, and M) a read-only-memory (ROM) control storage unit, and the microcode control logic. The E register stores 16-bits of data to be supplied to the microcode control logic. Fields in this register correspond to the microcode instruction word format and specify the instruction code, addressing mode, general register (RI through R7), index register, and occasionally a literal operand. The S register is a 12-bit counter that sequences microsteps, addresses the ROM control storage and is under control of the microcode word. The M register stores the 36-bit microcode that specifies action-a of the current microstep as well as control of the next microstep. The read-only-memory control storage unit contains microcode control words which are stored in ROM'S. The ROM's form a 36-bit, 256-word read-only-memory consisting of nine 256 by 4-bit LSI microcircuits. The 36-bit microcode word contains 13 fields for specification Of control functions within the Processor and selection of operands. A variety of conditional test and skip or branch microsteps are provided in the the field allowing conditional coding to minimize the number of microsteps required per function. 'The microcode control Logic contains buffers, delay circuitry, **clock generators, and gating necessary to control access to the ROM and controls signal transfers to the aritmetic register section. This section** also provides a ""look ahead" feature that allows the CPU, under macrocode control, to access the next microstep while executing the present step. Also includes in the microcode control logic is a control register that controls the CPU halt and run modes of operation.

5-755. CPA (80331230-000) (see figure 118). The CPA (AlA3A7) contains eight unique types of IC's (type SN74150P, SN74153N, SN74170N, SN74174N, SN74175N, SN74181, SN74182N, and SM74198N). The applicable paragraph describing these unique IC's are listed in table 5-1. The CPA in conjunction with a matched CPB form the CPU which is used to process data that is received from either Core Memory or Processor modules under control of stored software programs. The CPA contains the INFIBUS interface and arithmetic register sections of the CPU. The INFIBUS interface section consists of INFIBUS access logic and three registers (address, receive, and transmit). The INFIBUS access logic provides interface between the INFIBUS and CPU by providing control logic as well as address recognition logic. The three registers are gated to the arithmetic register section for logical or arithmetic operations. The arithmetic logic section consists of a multiplexer, arithmetic logic unit, and a register file. The multiplexer selects an operand from one of three registers or a 16-bit input data word. The 16-bit input data word is separated into four, 4-bit fields. Each field is individually enabled or disabled as an input to the arithmetic logic unit under microcode control. The arithmetic logic unit responds to commands from the CPB microcode word. These commands specify which one of 16 logical operations or which one of 16 arithmetic operations is to be performed. The register file consists of 12 16-bit registers.

5-756. CORE MEMORY CONTROLLER (80331010-000) (see figure 119). The Core Memory Controller (AlA3A8) contains two unique type of IC's (type SN74175N and SN74138N). The applicable paragraph describing these unique IC's are listed in table 5-1. The Core Memory Controller interfaces the Core Memory with the Processor INFIBUS. Under the control of the Processor, the Core Memory Controller determines whether the Core

Memory will operate in the clear/write or read/restore mode.

5-757. AUTOLOAD (80331150-000) (see figure 120). The Autoload (AlA3A9) contains three unique types of IC's (type SN7496, SN74100, and SN74157N). The applicable paragraph describing these unique IC's are listed in table 5-1. The Autoload contains a fixed, stored executive program that is used to reload the Core Memory in the event the program is lost. The Autoload is initiated by the autoload pulse (ATLD) which is generated by the Program Maintenance Panel when the autoload, atld, switch is touched, at power recovery, or power turn on if enabled by PRAL. PRAL is asserted by a switch located behind the Program Maintenance Panel. It allows autoload to occur automatically at power turn on or power recovery.

5-758. PARALLEL I/O (80331180-000) (see figure 121). The Parallel I/O (AlA3AlO) contains five unique types of IC's (type SN74153N, SN74157N, SN74174N, N8202N, and N8203N). The applicable paragraph describing these unique IC's are listed in table 5-l. The Parallel I/O provides interface between the Processor INFIBUS and the Alarm Control and VF Comm Link function, providing parallel input and output data lines. Operating in the slave mode only, the Parallel I/O recognizes its register addresses on the INFIBUS and receives or transmits data to or from one of its three registers; data (16 bits), status (12 bits) and control (6 bits).

5-759. TTY CONTROLLER (80331140-000) (see figure 122). The TTY Controller (AlA3A11) contains seven unique types of IC's (type SN7493A, SN74150P, SN74153N 5N74163N, SN74175N, SN74197N and SN74198N). The applicable paragraph describing these unique IC's are listed in table 5-1. The TTY Controller provides asynchronous interface between the Processor INFIBUS and the ASR TTY Function in the Switch Group on KSR TTY Function in the ACOC Group. It operates in the byte mode with a data rate of 110 baud. Data is transferred between the TTY Controller and INFIBUS as a parallel 8-bit byte, and between the TTY Controller and TTY Function serially on a single data input line and a single data output line. There are three addressable registers in the TTY controller, data (8 bits), control (6 bits), and status (4 bits). The data register receives and contains the data to be transferred. The control register specifies the current operation commands and the status register stores the TTY Controller and TTY Function status.

5-760. MODEM CONTROLLER 1 (80331210-000) (see figure 123). The Modem Controller 1 (AlA3A12) contains seven unique types of IC's (type SN7493A, SN74150P, SN74153N, SN74163N, SN74175N, SN74197N, and SN74198N). The applicable paragraph describing these unique IC's are listed in table 5-l. Modem Controller 1 provides asynchronous interface between the Processor INFIBUS and VF Comm Link 1. It operates in the byte mode with a data rate of 1200 baud. Data is transferred between Modem Controller 1 and INFIBUS as a parallel 8-bit byte and between the Modem Controller 1 and VF Comm Link 1 serially on a single data input line and a single data output line. There are three addressable registers in Modem Controller 1; data (8 bits), control (6 bits), and status (4 bits). The data register receives and contains the data to be transferred. The control register specifies the current operation commands and the status register stores Modem Controller 1 and VF Comm Link I status.

5-761. BLOCK TRANSFER ADAPTER (80331120-000) (see figure 124). The Block Transfer Adapter (AlA3A13) contains four unique types of IC's (type SN74153N, SN74157N, SN74163N, SN74191). The applicable paragraph describing these unique IC's are listed in table 5-1. The Block Transfer Adapter controls the Mag Tape Controller which transfer blocks of data directly to and from the Processor and Mag **Tape units.** Operating in the slave mode it receives initiating control words or transmits status information when

addressed by the Bus Controller. In the master mode it initiates direct data transfers on the INFIBUS when signalled by the Mag Tape Controller. Four registers, control, address, block length and status are contained in the Block Transfer Adapter for controlling and executing block transfers. The control register identifies the operation to be performed as an input (read) or an output (write) transfer operation. The address register holds the Core Memory or Mag Tape unit address to or from which data is to be transferred, and is incremented by a one after each byte or two after each word transfer. The word or byte count of the block to be transferred is stored in the block length register and decremented by one for each byte or word transfer. The status register indicates and stores the status of the Block Transfer Adapter. This register also has the same address as the status register in the Mag Tape Controller.

5-762. MAG TAPE CONTROLLER (80331130-000) (see figure 125). The Mag Tape Controller (A1A3A14) contains five unique types of IC's (type SN74153N, SN74157N, SN74174N, N8202N and N8203N). The applicable paragraph describing these unique IC's are listed in table 5-1. Controlled by the Block Transfer Adapter, the Mag Tape Controller, a parallel I/O, transfers blocks of data to and from the Core Memory and Mag Tape units, via the Processor INFIBUS and Formatter. The Mag Tape Controller provides 16 input and output parallel data lines operating in a half duplex mode. Operating in slave mode only the Mag Tape Controller recognizes its register addresses on the INFIBUS and receives or transmits data into or from one of its three registers, data (16 bits), status (12 bits) and control (6 bats).

5-763. I/O CONTROLLER (80330090-000) (Switch Group) (see figure 126). The I/O Controller (A1A3A15) contains four unique types of IC's (Type SN7442N, SN74138N, SN74174N, SN74175N, SN74178 and 9614). The applicable paragraph describing these unique IC'S are listed in table 5-1. The I/O Controller determines whether the Call Combiner Logic, Register Sendor Junctor, or Rapid Memory Reload function has access to the Processor INFIBUS. The I/O Controller is used only in the Switch Group Processor.

5-764. PRINTER CONTROLLER (80331280-000) (see figure 127). The Printer Controller (AlA3A15) contains seven unique types of IC's (type SN7493A, SN74150P, SN74153N, SN74163N, SN74175N, SN74197N, and SN74198N). The applicable paragraph describing these unique IC's are listed in table 5-l. The Printer Controller provides asynchronous interface between the Processor INFIBUS and the RO TTY function with a data rate of 110 baud. Data is transferred between the Printer Controller and INFIBUS as a parallel eight bit byte, and between the Printer Controller and RO TTY Function serially on a single data input line and a single data output line. There are three addressable registers in the Printer Controller data (8 bits), contro1 (6 bits), and status (4 bits). The data register receives and contains the data to be transferred, the control register specifies the current operation commands and the status register holds Printer Controller and RO TTY Function status. The Printer Controller is used only in the ACOC Group Processor.

5-765. MODEM CONTROLLER 2 (80331190-000) (see figure 128). The Modem Controller 2 (A1A3A16) contains seven unique types of IC's (type SN7493A, SN74150P, SN74153N, SN74163N, SN74175N, SN74197N, and SN74198N). The applicable paragraph describing these unique E's are Lasted in table 5-l. The Modem Controller 2 provides asynchronous interface between the Process INFIBUS and VF Comm Link 2 function with a data rate of 1200 baud. Data is transferred between the Modem Controller 2 and INFIBUS as a parallel 8-bit byte, and between the Modem Controller 2 and VF Comm Link 2 serially on a single data input line and a single data output line. There are three addressable registers in the Modem Controller 2 data (8 bits), control (6 bits), and status (4 bits). The data register receives and contains the data to be transferred, the control register specifies the

current operation commands and the status register holds Serial I/O and VF Comm Link 2 status. The Modem Controller 2 is used only in the ACOC Group Processor.

5-766. PBI (8033 1250-000) (see figure 129). The PBI (Switch: AlA3A20, ACOC: AlA3A17) contains three unique types of IC's (type SN74161J, SN74175N, and NS74197N). The applicable paragraph describing these unique IC's are listed in table 5-l. The PBI, in conjunction with the PCB and SWB, forms the Program Maintenance Panel. The PBI provides the logic and interface between the Program Maintenance Panel and INFIBUS enabling the Program Maintenance Panel to gain INFIBUS access. The PBI provides control logic, timing, micro operations, and bus driver/receiver circuits. The timing circuits consist of clock, state generation and a control register. The Micro operations circuit controls INFIBUS access logic, address recognition, and address comparison.

5-767. PCB (80331260-000) (see figure 130). The PCB (Switch: AlA3A21, ACOC: AlA3A18) contains eight unique types of IC's (Type SN7493A, SN74150P, SN74154N, SN74157N, SN74175N, SN74198N, N8266B, and HD0165). The applicable paragraph describing these unique IC's are listed in table 5-1. The PCB in conjunction with the PCI and SWB forms the Maintenance Panel which provides the logic and interface between the Program Maintenance Panel and INFIBUS. The PCB provides the Program Maintenance Panel SWB switches and indicators with the necessary registers and drivers. The PCB sends and receives data to and from the INFIBUS via strobed bus driver/receivers. Also contained in the PCB are switch identification, shift register, address recognition and address comparison circuits.

5-768. SWB (90331080-000) (see figure 131). The SWB in conjunction with the PBI and PCB forms the Program Maintenance Panel which provides a means of manual access and indication to all CPU and other modules internal registers for program control and maintenance. Contained in the SWB are 62 momentary switches, 65 light emitting diode (LED) indicators, and three hidden accessible toggle switches for program debugging. When enabled, it is capable of sending switch closures to the Program Maintenance Panel logic which drives the indicators and provides interface with the INFIBUS. Operating in the master mode it can communicate via the INFIBUS with any other addressable system module such as CPU, memories, or peripheral device controllers. In the slave mode other systems modules can access the Program Maintenance Panel via the INFIBUS. If data on the INFIBUS that is addressed to the Program Maintenance Panel, conflicts with information stored in the Program Maintenance Panel, the data from the Program Maintenance Panel is always retained.

5-769. CM MIA (80332060-000) (see figure 132). The CM MIA (AlA8Al) contains the timing and control logic, address register and reset circuits of the Core Memory. The timing and control logic receives the control signals from the Processor and generates internal timing signals which control all functions in the Core Memory. The address register receives 15 address bits from the Processor. Bits 0 to 6 are X address and bits 7 to 12 are Y address. Bits 13, 14 and 15 at-c decoded to produce CM BSM select signals. The reset circuit prevents accidental loss of data in event of power failure, providing an orderly shut down sequence and ensuring that the cycle in progress is properly completed.

5-770. CM MIB (80331370-000) (see figure 133). The CM MIB (AlA8A2) provides the data register and zone control circuits of the Core Memory. The data register consists of 18 flip-flops, one for each system bit. Gated by signal +SAS and reset by timing signal +RDR the data register receives and stores information from the CM MMA core memory stack until it is strobed to the data output lines and/or restored in the core memory stack. The data register also stores incoming information from the data input lines during write operations. Zone control is operative during the clear/write write cycle and

allows selective clear/write and read/ restore operations to be performed in one or both bytes within a given word.

5-771. CM MBA (80331090-000) (see figure 134). The CM MBA (Switch: AlA8A3A1, AlA8P4A1, AlA8A5A1, AlA8A6A1, ACOC: AlA8A3A1, AlA8A4Al) contains the inhibit drivers and sense gates circuits of the CM BSM. The inhibit circuit is operative only during the restore portion of read/restore mode and during the write portions of the clear/write mode. The inhibit circuit is used when a zero is to be written. Current is driven through the sense/inhibit line, in the opposite direction from the current in the Y line, and of equal amplitude to that of the Y current. This causes the Y current to be algebraically neutralized, core turn over does not occur, and the core is left in the "0" state. The sense gates operate during the read cycles and receive information from the CM MMA core memory stack via strobed amplifiers. The sense gates are controlled by the CM MIB.

5-772. CM MMA (80331110-000) (see figure 135). The CM MMA (Switch: AlA8A3A2, AlA8A4A2, AlA8A5A2, AlA8A6A2. ACOC: AlA8A3A2, AlA8A4A2) contains the diode matrices and core memory stack of the Core Memory. The X and Y diode matrices select individual X and Y lines in the core memory stack. The core memory stack consists of 18 mats of 8K (8192) cores each. Address information on X and Y lines is threaded through given cores at right angles to each other on all 18 mats so that a given address location specifies one core on each mat. Data information on sense/inhibit line is threaded through all the cores on a given mat parallel to address Y nine. When current is driven along this Bane in the opposite direction from the direction of the Y current, the Y current is algebraically cancelled.

5-773. CM MSA (80331080-000) (see figure 136). The CM MSA (Switch: AlA8A3A3, AlA8A4A3, AlA8A5A3, AlA8A6A3. ACOC: AlA8A3A3, AlA8iUA3) contains one unique type of IC (type SN74145). The applicable paragraph describing this unique IC is listed in table 5-1. The CM MSA provides the control and buffer logic, address decoding and switching, and X and Y current source circuits of the C M BSM. The control and buffer logic receives a select signal from CM MIA enabling it to control address switching and data flow from CM MMA core memory stack to CM MIB data register. The address decoding and switching circuitry receives the address information from the CM MIA address registers and decodes this information to turn on one set of X switches and one set of Y switches, resulting in current drive through one X line and one Y line in each plane of the CM MMA core memory stack. X and y current sources for X and Y line drive are generated by a voltage regulator. The voltage regulator, an operational amplifier and related circuitry, supplies approximately 3 volts dc.

5-774. INTEGRATED CIRCUIT DESCRIPTIONS.

5-775. HD-0165, KEYBOARD ENCODER (see figure 137). The HD-0165 Keyboard Encoder is a 16 line to 4-bit parallel encoder. It is used with manual data entry devices such as a typewriter and codes each key input to a 4-bit binary code. The HD-0165 has 16 input lines which are normally wired through key switches of a manual data entry device to +Vcc. The 4-line outputs provide the binary code for each of the input lines. The HD-0165 features a strobe output that is normally used to gate the encoded signal to other circuitry. The Strobe output may be conditioned by external components to eliminate switch bounce or skew in output propagation de lays. The output is high with no input and goes low with any of the input lines being high. The HD-0165 also features a KEY ROLLOVER (KRO) output that is always high except when 2 or more input lines go high indicating the data output is not valid. By using the truth table provided and proper wiring of the input line, any four-bit code can be produced for a particular key.

5-776. N8202N, 10-BIT BUFFER REGISTER (see figure 138). The N8202N is a 10-bit

buffer register made up of ten D-type flip-flops. The flip-flops are simultaneously clocked (pin 1) and reset (pin 23). The logic states at the D inputs (pins 2 through 11) will appear at the Q outputs (pins 13 through 22) after the high-to-low transition of the clock input. The flip-flops will show the data at the Q outputs till reset or power recycled without altering their states. The table provided applies to all 10 flip-flops.

5-777. N8203N, 10-BIT BUFFER REGISTER INVERTED INPUTS (see figure 139). The N8203N is a 10-bit buffer register consisting of 10 D-type flip-flops. The logic state the D inputs (pins 2 through 11) will invert and appear at the Q outputs (pins 13 through 22) after a high-to-low transition of the clock input (pin 1). All 10 flip-flops are reset, Q outputs go low, when the reset input (pin 23) goes low regardless of the clock and D inputs. The data at the Q outputs will not alter till the flip-flops are reset or load with other data. The table provided applies to all 10 flip-flops.

5-778. N8235N, 2-INPUT, 4-BIT DIGITAL MULTIPLEXER (see figure 140). The N8235N is a 2 bit binary decoder and multiplexer which operates as four 2-bit parallel to serial data converters. Depending on the level of the data select inputs, SO and Sl (pins and 9), a specific gate is enabled to p its corresponding data inputs (pins 1, 2, 5, 6, 10, 11, 14, and 15) to the data outputs (pins 3, 4, 12 and 13) as shown in the associated truth table. When both select inputs are high all the data outputs are high. When both data inputs are tied together, the data output will provide either the true (non-inverted) or compliment (inverted) of the data input.

5-779. N8264N, 3-INPUT, 4-BIT DIGITAL MULTIPLEXER (see figure 141). The N8264N IS triple 2-bit binary decoder which operates as four 3-bit parallel to serial data converters. Depending on the binary value of the channel selects, S0 and Sl (pins 16 and 17) a specific gate is enabled to pass its corresponding data inputs (pins 1 through 6 and 18 through 23) to the output gates (see associated truth table). When the data compliment (pin 16) is low the selected non-inverted input is passed to the data output (pins 10, 11, 13, and 14) if the output enable inputs (pins 7, 8 and 9) are high. When the data compliment is high the selected inverted data input is passed to the data output if the output enable inputs are high. When any one of the output enable inputs goes low, all the data outputs go high. When both channel selects are low and the output enable input are all high, the data output follow the data compliment levels.

5-780. N8266B, 2-INPUT, 4-BIT DIGITAL MULTIPLEXER (see figure 142). The N8266B is a 2-bit binary decoder and multiplexer which operates as four 2-bit parallel to serial data converters. Depending on the level of the data select inputs, SO and Sl (pins 7 and 9), a specific gate is enabled to pass its corresponding data inputs (pins 1, 2, 5, 6, 10, 11, 14, and 15) to the data outputs (pins 3, 4, 12 and 13) as shown in the associated truth table. When both select inputs are high all the data outputs are high. When both data inputs are tied together the data output will provide either the true (non-inverted) or compliment (inverted) of the data input.

5-781. P3205, HIGH SPEED 1 OUT OF 8 BINARY DECODER (see figure 143). The P3205 is a high speed decoder used in high speed data routing applications. It generates one of eight lines (outputs 00 through 07) that is dependent on the conditions at the three enable inputs (E1, E2, and E3) and the select inputs (Al, A2, and A3). The enable inputs are three active low to reduce the need for external gates and inverters when expanding. The enable inputs **must** all be low to enable the decoder. When the decoder is enabled, it decodes the three select input causing the decoded output (00 through 07) to go low.

5-782. P3404, HIGH SPEED 6-BIT LATCH (see figure 144). The P3404 contains six high speed latches organized as independent 4-bit and 2-bit latches. They are designed for use as memory data registers, address registers, or other storage elements. Data applied to the data inputs Dl through D6 is

stored in the associated latch. When the write 1 input W 1 goes low, the data stored in the four latches is coupled to the data outputs 01 through 04. When the write 2 input W2 goes low, the data stored in the two latches is coupled to the data outputs 05 and 06. If Wl and/or W2 is held low the associated latches act as high speed inverters.

5-783. SN7442N, BCD TO DECIMAL DECODER (see figure 145). The SN7442N is a decoder which translates a 4-bit BCD code into on of ten corresponding decimal outputs. Full decoding of a valid input number (0 to 9) ensures that one specific output is low, while all outputs remain off (high) for all invalid input (10 through 15) conditions (see associated truth table).

5-784. SN7493A, DIVIDE BY 2, 8 or 16 BINARY COUNTER. (see figure 146). The SN7493A is a four master-slave flip-flop binary counter capable of a divide by 2, 8 or 16 count. 3 of the flip-flops are connected for .a divide by 8 count using input B (pin I) and outputs B, C, D (pins 9, 8 and 11). The flip-flop with input A (pin 14) is a divide by 2 stage and when output A (pin 13) is connected to input B, a divide by 16 stage is formed using input A for the input count. All four master-slave flip-flops are tied to a common gated reset line which inhibits the count and simultaneously resets the flip-flops.

5-785. SN7496, 5-BIT SHIFT REGISTER (see figure 147). The SN7496 shift register consists of five W-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. With both inputs and outputs of the five flip-flops accessible, parallel-in/parallel-out or serial-in/serial-out operations may be performed. win the flip-flops are simultaneously set to a low output level with a Bow-level to the clear and preset enable inputs. Clearing is independent of the level of the clock input. The register can be parallel loaded by using theclear input in conjunction with the preset inputs. After the stages are cleared to low level outputs, data is loaded through preset inputs A, B, C, D, and E (pins 2, 3, 4, 6, and 7) with a high level load pulse applied to the preset enable inputs. Presetting is also independent of the clock input level. The data then can be read out in parallel through the outputs QA, QB, QC, QD and QE or the register can be clocked with the data taken out in serial out of Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The serial input provides the data to the first R-S flip-flop, which the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset enable inputs low when clocking occurs.

5-786. SN74100, 8-BIT BISTABLE LATCHES. (see figure 148). The SN74100 contains eight latches used for temporary storage of binary data between processing units and input/output or indicator units. The SN74100 has two enable inputs (pins 12 and 23) each enabling a group of four latches. Four bits at a time can be latched or the enable inputs can be tied together to latch eight bits at a time. The following description is applicable to all eight latches. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the **information,** that was set up at the data input at the time the transitnon occurred, is retained at the Q output until the enable goes high.

5-787. SN74138M, 3 Line-to-8 Line DECODER/DE MULTIPLEXER. (see figure 149). The SN74138N is a high-speed decoder/demultlplexer used in high speed 0 a routing applications. It *generates one or eight lines that is dependent on the* conditions at the three enable inputs and three binary select inputs, The enable inputs are two active-low, G2A and G2B, and one active high, Gl, to reduce the need for external gates or inverers when expandang. In the decoding mode, inputs G1, G2A and G2B (pins 6, 4, and 5) are enabled and a three bit binary data input is applied to the select inputs A, B, and C (pins 1, 2, and 3). The three bit data

is decoded to select one of eight lines YO through Y7 (pins 7, 9 through 15). In the demultiplexing mode, one of the enable inputs is used for the data input and the select inputs routes the data through to the selected line.

5-788. SN74145, BCD-TO-DECIMAL DECODER/DRIVER. (see figure 150). The SN74145 is a binary-coded-decimal (BCD) to decimal decoder with each output capable of sinking a relative large current. Only valid BCD inputs are decoded and for a invalid BCD input, the outputs will be high. The valid BCD data is applied to inputs A, B, C, and D (pins 12, 13, 14 and 15) and decoded to select one of ten high-breakdown output transistors (pins 1 through 7, 9, 10 and 11) where each are capable of driving a relative large load. The SN74145 is usually used as lamp drivers or relay drivers.

5-789. SN74150P. DATA SELECTOR/ MULTIPLEXER (see figure 151). The SN7415OP is a 4-binary decoder and multiplexer which operates as an 16-bit parallel to serial converter. Depending upon the binary value of the input data select (pins 11 and 13 through 15), a specific gate is enabled to pass its corresponding data input (pins 1 through 8 and 16 through 23) to the W output (pin 10) in the complement format. This selection and multiplexing of 16 data bits is performed whenever the strobe input (pin 9) is low (see associated truth table.

5-790. SN74151AJ. DATA SELECTOR/ MULTIPLEXER (see figure 152). The SN74151AJ is a 3-bit binary decoder and multiplexer which operates as an 8-bit parallel to serial data converter. Depending upon the binary -value of the input data select (pins 3 through 11), a specific gate is enabled to pass its corresponding data input (pins 1 through 4 and 12 through 15) to the W and Y outputs (pins 6 and 5) in both complements and non-complement format. This selection and multiplexing of eight data bits is performed whenever the strobe input (pin 7) is low (see associated truth table).

5-791. SN74153N, DUAL 4 LINE-TO-1 LINE DATA SELECTORS/MULTIPLEXERS (see figure 153). The SN74253N is a 2-bit binary decoded dual 4-bit parallel to serial converter. The select inputs (pins 2 and 14) select each of the 4 input lines of both multiplexers simultaneously. Each multiplexer is provided with STROBE inputs (pins 1 and 15) to STROBE (Enable) each of the multiplexers individually. The truth table provided show the SELECT INPUT (B and A) codes for each input lines.

5-792. SN74154N. 4 LINE-TO-16 LINE DECODERS/DEMULTIPLEXERS (see figure 154). The SN74154 is a decoder/multiplexer which decodes 4-bit binary coded inputs into one of sixteen outputs OR demultiplexes data from one of two strobe inputs to one of the sixteen outputs as selected by the 4-bit binary-coded input. When both strobe inputs are low, the output gates are enabled and the binary-coded decimal input is decoded and the selected output line goes low. When either strobe is high, all of the output lines are also high and when the other strobe input line goes low, the output line as selected by the 4-bit binary-coded inputs also goes low. When both strobe input lines are high all of the output lines are high (see associated truth table).

5-793. SN74157N. QUADRUPLE 2 LINE-TO-l LINE DATA SELECTORS/MULTIPLEXERS. (see figure 155). The SN74157N is a quadruple 2-bit decoder which operates as a four 2-line to serial data converters. A separate strobe input is provided that strobes (enables) all four 2-line to serial converters simultaneously. A 4-bit word is selected from one of two sources (A and B inputs) and presented at the outputs when strobcd (see associated truth table).

5-794. SN74161J, SYNCHRONOUS 4-BIT COUNTER (see figure 156). The SN74161J is a presettable synchronous binary counter. Presetting or loading of the **counter** is accomplished when a low-to-high trasistion is applied to the **clock** input (pin 2) at a time when a binary value from 0 to 15 is received at the data inputs

(pins 3 through 6) and the load input (pin 9) is low. This action causes the four J-K flip-flops to store the bin binary value applied at the data inputs. Once the load input goes high and the enable inputs (pins 7 and 10) are both received at high levels, each successive low-to-high transition of the clock input increments the counter from the previous binary value to the next binary value. At each count. of 15 (all four flip-flops are set), a ripple carry output (pin 15) is issued at a high level; at the next count (zero) the ripple carry output goes low and remains low until the counter is again incremented to a count of 15. Thus a positive overflow carry pulse is generated 1 count in every 15 and can be used to enable successive cascaded counter stages. Termination of the counting process is provided by an asynchronous clear input (pin 1). Once the clear input goes low, all four flip-flops are reset (count of zero), regardless of the levels of the clock, load or enable inputs.

5-795. SN74163N, SYNCMRONOUS 4-BIT COUNTER (see figure 157). The SN74163N is a presettable synchronous counter. Presetting or loading of the counter is accomplished when a low-to-high transition is applied to the clock input (pin 2) at a time when a binary value from 0 to 15 is received at the data inputs (pins 3 through 6) and the load input pin is low. This action causes the four J-K flip-flops to store the binary value applied to the data inputs. Once the load input goes high and the enable inputs (pins 7 and 10) are both received at high levels, each successive low-to-high transition of the clock input increments the counter from the previous binary value to the next binary value. At each count of 15 (all four flip-flops are set), a ripple carry output (pin 15) is issued at a high level; at the next count (zero) the ripple carry output goes low and remains low until the counter is again incremented to a count of 15. Thus a positive pulse is generated one count in every 15 and can be used to enable successive cascaded counter stages. Termination of the counting process is provided by a synchronous clear input (pin 1). When the clear input goes low, the first low-to-high transition of the clock input causes all four flip-flops to reset (count of zero), regardless of the load or enable inputs.

5-796. SN74170N, 4-BY-4 REGISTER FILE (see figure 158). The SN74170N is a 4-word, 4-bit register file and decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location. The four data inputs (pins 1, 2, 3, 15) are used to supply the 4-bit word to be stored. The write address inputs (pins 13 and 14) in conjunction with the write enable (pin 12) determine the location of the word to be stored (see write truth table). Data applied to the data inputs should be in its true form. If a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal latch gate inputs are high. When this condition exists, data at the data input is transferred to the latch output. When the write enable line is high the data inputs are inhibited and their levels cause no change in the information stored in the internal latches. The read inputs (pins 4 and 5) enable specific gates that determine which word is to be selected for read-out. The read enable input (pin 11) enables gates that pass the selected word to the outputs (pins 6, 7, 9 and 10). When the read enable input is high, all data outputs are high and remain high.

5-797. SN74174N, HEX D-TYPE FLIP-FLOPS WITH CLEAR (see figure 159). The SN74174N is a 6-bit storage register. Data at the inputs (pins 3, 4, 6, 11, 13, 14) is transferred to the Q outputs (pins 2, 5, 7, 10, 12, 15) on the positive-going edge of the clock input (pin 9). Resetting of the register is provided by an asynchronous clear input (pin 1). Once the clear input goes low, all six flip-flops are reset, regardless of the levels of the clock and data inputs.

5-798. SN74175N, QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR (see figure 160). The SN74175N is a 4-bit storage register. Data at the inputs (pins 4, 5, 12, and 13) is transferred to the Q outputs (pins 2, 7, 10 and 15) and the compliment is transferred to the Q outputs (pins 3, 6, 11 and 14 on the positive-going edge of the clock input (pin 9). Once the clear input (pin 1) goes low, all four flip-flops are reset, regardless of the levels of the clock and data inputs. The four inputs are wired to the D inputs of each flip-flops and they are clocked in parallel with clear input also. With a 4-bit input, each bit is loaded to a flip-flop on the positive edge of the clock input and the flip-flops will hold their loaded state till cleared or power recycled. The output can be taken of the Q outputs of each flip-flop and also the complement of the Q outputs without altering the state of each flip-flop. The truth table provided applied to each flip-flop.

5-799. SN74178, 4-BIT PARALLEL ACCESS SHIFT REGISTER. (see figure 161). The SN74178 is a d-c coupled high frequency (39 MHZ) 4-bit shift register able to operate in three modes; synchronous parallel load, right-shift, and hold. The clock input responds to a negative going trigger and the four flip-flops are directly cleared. It also has the D flip-flop providing Q output. Parallel loading is accomplished by taking the shift input low, applying the four bits of data, and taking the load input high. The data is loaded into the associated flip-flop synchronously and appears at the outputs after a high-to-low transition of the clock. During loading, serial data flow is Inhibited. Shift right IS also accomplished on the falling edge of the clock pulse when the shift input is high regardless of the level of the load input. Serial data for this mode is entered at the serial data input. When both the shift and load inputs are low, clocking of the register can continue; however, data appearing at each output is fed back to the flip-flop input creating a mode in which the data is held unchanged. Thus, the system clock may be left free-running without changing the contents of the register (see associated truth table).

5-800. SN74181, ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR. (see figure 162). The SN74181 is an Arithmetic Logic Unit (ALU) capable of performing 16 binary operations of two 4-bit words. The 16 operations ***are*** selected by the four function-select lines (SO, Sl, S2, S3) with mode control input (M) high for logic operations and low for arithmetic operations. The logic-function mode provides Exclusive-OR, Comparator, AND, NAND, OR, NOR, and ten other logic operations. The arithmetic mode provides addition, subtraction, shift operand A one position, magnitude comparator, and twelve other arithmetic operations. Two cascaded outputs (pins 15 and 17) are available for direct connection with a SN74182N (look-ahead carry generator) for high speed look-ahead carry functions. Ripple-carry input (Cn) and a ripple-carry output (Cn+4) are provided if high speed carry operation is not needed. The subtracting function of the ALU is performed by l's complemented addition and with l's complement subtrahend being generated internally. In the Comparator mode, the ALU should be in the subtract mode with ripple carry (Cn) high. In this mode that A-B outputs (pin 14) is internally decoded from the function outputs (FO, F1, F2, F3). With two words of the same magnitude applied to the A and B inputs, the A=B output will go high indicating equality. The 16 functions of the two Boolean variables (A and B input words) that are selected by the four function-select lines are shown by the table with active high data inputs.

5-801. SN74182N, LOOK-AHEAD CARRY GENERATOR (see figure 163). The SN74182N is a high speed, look-ahead carry generator. Used in conjunction with four Arithmetic Logic Units (ALU's) it is capable of anticipating a carry across the ALU group providing high speed carry operations. The SN74182N provides carry, generate-carry, and propagate-carry functions as indicated the pin designation table. The active low propagate-carry output P

(pin 7) is provided by OR gated propagate-carry inputs (POPl,P2,P3). The active low generate-carry output, G (pin 10) is provided by OR'd AND gated generate-carry inputs (GO, Gl, G2, G3). The carry outputs are provided by NCR'd AND gated generate-carry inputs, propagate-carry inputs, and carry input (Cn) that is generated by an up-stage ALU-SN74182N stage. Carry output Cn+x (pin 12) is derived from NCR'd AND gated carry input (Cn), generate-carry input (GO), and propagate-carry input (PO). Carry output Cn+y (pin 11) is derived from NOR'd AND gated generate-carry inputs (GO and Gl) and carry input (Cn). Carry output Cn+z (pin 9) is derived from NOR'd AND gated generate-carry inputs (Go, Gl, G2) and carry input (Cn). With the outputs from the ALU's being in negated form, the Boolean expressions of each output given holds true.

5-802. SN74191, SYNCHRONOUS UP/DOWN COUNTER WITH UP/DOWN COUNT MODE CONTROL (see figure 164). The SN74191 is a presettable, synchronous, up/down, binary counter. Presetting or loading of the counter is accomplished when a high-to-low transition occurs on the load input (pin 11) when a binary value from 0 to 15 is on the data inputs (pins 1, 9, 10 and 15). This action causes the four J-K flip-flops to store the binary value applied at the data inputs. If the enable input (pin 4) is low and the load input goes high and if the down/up input (pin 5) is Pow each successive high-to-Bow transition of the clock (pin 14) increments the counter from the previous binary value to the next higher binary value, id the down/up input is high each successive high-to-low transition of the clock increments the counter from the previous binary) value to the next lower binary value. At each count of 15 (all four flip-flops are set) a high-level max/min output (pin 12) pulse, one clock period wide; and a low-level ripple clock (pin 13), one-half clock period wide, are issued. At the next count of (0 or 14) the max/min output goes low and the ripple clock output goes high until the counter is again incremented to a count of 15. Thus a positive and a negative overflow carry pulse is generated 1 count in every 15 and they can be used to enable successive cascaded stages. When the enable input (pin 4) goes to a high level both up and down counting is inhibited and the counter holds the binary value of the last count. When the enable input goes to a low level the counter. begins to count again, beginning with the stored last count (no reset).

5-803. SN74197N, 50/30 MHZ PRESETTABLE BINARY COUNTER/LATCHES (see figure 165). The SN74197N is a 4-bit presettable binary counter consisting of four d-c coupled, master-slave flip-flops which are internally connected to provide a divide by two counter and a divide of eight counter. Presetting or loading of the counter is accomplished by placing a low-level on the count/load input (pin 1) when the binary value from 0 to 15 is on the data inputs (pins 3, 4, 10 and 11). This action causes the four flip-flops to store the binary value applied to the data inputs and the outputs (pins 2, 5, 9 and 12) will change to agree with the data inputs regardless of the state of the clocks. Once the count/load input goes to a high-level each successive high-to-low transition of the clocks (pins 6 and 8) increments the counter. Termination of the counting process is provided by an asynchronous clear input (pin 13). Once the clear input goes low, all four flip-flops are reset (count of zero) regardless of the clocks and the count/load inputs- As the output (pin 5) of the first flip-flop is not connected to the succeeding flip-flops, the counter can operate in two independent modes. When used as a 4-bit binary counter the output (pin 5) of the first flip-flop must be externally connected to the clock 2 input (pin 6). Simultaneous division by 2, 4, 8, and 16 are performed at the outputs (pins 2, 5, 9, and 12). When used as a 3-bit binary counter the output (pin 9) of the second flip-flop becomes the least significant bit and the clock 2 input is divided by 2, 4, and 8 at the outputs (pins 2, 9 and 12). This counter may also be used as 4-bit latches by using the count/load as the strobe and entering data at the data inputs. The outputs will directly follow

the data inputs when the count/load is low and will remain unchanged when the count/load is high. When used as 4-bit latches the clock 1 and clock 2 input must be held inactive.

5-804. SN74198N, 8-BIT SHIFT REGISTER (see figure 166). The SN74198N is an 8-bit shift register that has four modes of operation, parallel load, shift right (Q_A toward Q_H), shift left (Q_H toward Q_A), and inhibit. Synchronous parallel loading by applying the eight bits of data (pins 3, 5, 7, 9, 15, 17, 19, and 21) and taking both mode control inputs, S_0 and S_1 (pins 1 and 23), high (see associated truth table). The data is loaded into the associated flip-flop and appears at the associated data output (pins 4, 6, 8, 10, 14, 16, 18 and 10) after the low-to-high-high transition of the clock input (pin 11). During loading serial data flow is inhibited. Shift right is accomplished synchronously with the low-to-high transitions of the clock when is high and Sl is low. Serial data for this mode is entered at the shift-right data input (pin 2). When S0 is low and 1 is high data shift left synchronously and new data is entered at the shift-left serial input (pin 22). When S_0 and S_1 are both low, clocking of the flip-flops is inhibited. When the clear input goes low, all 8 flip-flops are asynchronously reset regardless of the clock, mode control (S_0 and S_1), and data inputs.

5-805. SN75453, DUEL PERIPHERAL POSITIVE-OR DRIVER (see figure 167). The SN75453 is a dual high-speed peripheral-OR driver with the outputs of the logic gates internally connected to the bases of the NPN output transistors. The emitters of both transistors are internally tied to ground and brought out to pin 4. The collectors are open and each can be tied to a pull-up resistor to drive a line or both collectors may be tied together to a pull-up resistor for multiplexing operations (wired-OR). Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers and memory drivers.

5-806. U7B961455X, DUAL DIFFERENTIAL LINE DRIVER (see figure 168). The U7B961459X is a TTL compatible dual differential line driver. It is designed to drive transmission lines either differentially or single-ended, back matched or terminated. The output are similar tc TTL, with active pull-up and the pull-down split and brought out to adjacent pins. This allows multiplex operation (wired-OR) at the driving site in either the single-ended mode via the uncommitted collectors or in the differential mode by use of the active pull-ups on one side and the uncommitted collectors on the other. The two pairs of outputs are complementary, providing "NAND" and "AND" outputs when all three inputs are high.

5-807. U7B961559X DUAL DIFFERENTIAL LINE RECEIVER (see figure 169), The U7B961559X is a dual differential line receiver designed to receive differential digital data from transmission lines. A strobe is provided along with a 130 ohm terminating resistor (at the input) to enable the differential data to be processed. However, in most applications, the strobe input is tied to +VCC. The output has an uncommitted collector with an active pull-up available on an adjacent pin. When the positive input (pin 5 or 11) is 500 millivolts more positive than the voltage applied to the negative input (pin 7 or 9), the output (pin 1 or 15) goes low while the active pull-up (pin 2 or 14) goes high. Conversely, when the positive input is 500 millivolts more negative than the voltage applied to the negative input, the output (pin 1 or 15) goes high while the active pull-up (pin 2 or 14) goes low. Therefore, for a differential input, TTL logic is seen at the output.

S E C T I O N I I I

FUNCTIONAL OPERATION OF MECHANICAL ASSEMBLIES

MOT APPLICABLE

CHAPTER 6

MAINTENANCE

6-1. INTRODUCTION

6-2. This Chapter provides maintenance information for the Processor and Gore Memory. The level of information is based on the assumption that maintenance personnel have been trained on, and are familiar with this type of digital computer equipment. Section I Organization and Intermediate Maintenance, provides procedures to localize faults in a functional group to a specific PC card. Section II Special Maintenance, includes test procedures to isolate a PC card malfunction to individual component(s) (integrated circuit) level, Section III Performance Test Checks, describes overall test procedures for the Processor and Core Memory on a functional basis.

6-3. MAINTENANCE CONCEPT. The performance test checks in Section III should be performed at periodic intervals or whenever a trouble is suspected in the Processor and Core Memory. As a result of these checks, troubles can be isolated to a major functional group consisting of one or more PC cards and units (Bus Controller, CPA, CPB, CM BSM, etc.). Once the fault has been isolated to a functional group, the performance test standards in Section I should be used to localize the fault to a PC card or unit which can be immediately replaced with a known good PC card or unit to minimize equipment down time. If the minimum performance standards in Section I localize the trouble to one or two PC cards, the suspected PC cards should be substituted with known good PC cards, one at a time, until the trouble is corrected.

6-4. When time permits (e.g. during maintenance periods with the equipment off line), the defective PC card should be reinstalled in the equipment so that additional special maintenance as described in Section II can be performed to isolate the malfunction to a defective component or group of components.

6-5. After replacing the defective component (or group of components), reinstall the PC card in the equipment and repeat the applicable Section III procedure to verify that the PC card has been properly repaired.

6-6. USE OF TEST POINTS. A system of test point identification symbols are incorporated on the equipment schematics (contained in Technical Manual, Circuit Diagrams T.O. 31S5-4-308-3) to aid maintenance personnel in using the component tests in conjunction with the schematics to isolate problems.

a, A star encircled number -- ☆1 -- defines a major point of test that isolates a problem to a functional group. These test points are placed at critical input and outfit signal or logic control lines between functional groups; e.g., between the Processor and Core Memory.

b. Where a function comprises two or more PC cards, a secondary test point, an encircled capital Better -- (A) --, is used to identify a signal or logic control line which isolates the problem to a specific PC card.

c. An encircled capital letter and number -- (A1) --, defines a minor test point which is used to localize a malfunction to a defective component(s).

SECTION I

ORGANIZATIONAL AND INTERMEDIATE MAINTENANCE

6-7. GENERAL.

6-8. The organizational and intermediate maintenance procedures described are divided according to the Processor and Core Memory acceptance test tapes (GINS I, II, III, IV Test, Interrupt Test, Worst Pattern Memory Test, etc.). The procedures are provided in the form of test tables that contain performance standards (TTY print outs or visual indications) which indicate that a function is operating normally under the conditions specified.

6-9. MAINTENANCE SUPPORT EQUIPMENT.

6-10. Table 6-l lists the test equipment required to perform maintenance on the Processor and Core Memory. To permit substitution of suitable test equipment, when the listed test equipment is not available, the test paramenters (characteristics) and required accuracies for the test outlined in this chapter are also given.

6-11. PERFORMANCE TEST STANDARDS.

6-12. The performance test standards comprise tests relating to the Processor and Core Memory functions. These tests contain performance standards which, if unobtainable, isolate malfunctions to one or more replaceable PC cards. The tests are accomplished by use of an Acceptance Test Program (ATP) test tape. The test tape is comprised of 12 functional tests and a utility program listed below:

ATP Test	Function
BOS	Basic operating system (BOS) program; a collection of Programmer/Operator-oriented utility routines, and a command processing monitor.
GIN I	Performance test for CPA, CPU, and Bus Controller, Part I.
GIN II	Performance test for CPA, CPB, and Bus Controller, Part II.
GIN III	Performance test for CPA, CPB, and Bus Controller, Part III.
GIN IV	Performance test for CPA, CPB, and Bus Controller, Part IV.
Interrupt Test	Performance test for CPA, CPB, and Bus Controller Interrupt.
Memory Address	Performance test for Core Memory and Core Memory Controller, Part I.
Random Data	Performance test for Core Memory and Core Memory Controller, Part II.

ATP Test	Function
Worst Pattern Memory	Performance test for Core Memory and Core Memory Controller, Part III.
LF and Power Fail Restart	Perforance test for CPA, CPB, PBI, PCB, and Program Maintenance Panel.
Control Panel Test	Performance test for Program Maintenance Panel, FBI, and PCB.
Teletype 33/35	Performance test for TTY Controller and Printer Controller.
SUE Mag Tape (BTA)	Performance test for Mag Tape Controller and BTA.

Refer to paragraph 6-13 for above listed tests. For performance test standards for the Autoload, Parallel I/O, Modem Controller and I/O Controller, refer to paragraphs 6-17 through 6-20, respectively.

Table 6-1. Maintenance Support Equipment

EQUIPMENT IDENTIFICATION	CHARACTERISTICS	
Multimeter, AN/PSM-6	Resistance range:	0 to 30 megohms in 5 ranges.
	Dc volts range:	0 to 5000vdc in 8 ranges.
	Ac volts range:	0 to 1000vac in 7 ranges.
Electronic Frequency Counter, MIL-C-9988 Type IV	Frequency range:	0 to 60MHz
	Gate time:	1 usec to 10 sec in decade steps.
	Accuracy:	±1 count ± time base accuracy
	Imput resistance:	10 megohms ±3% on 150mv range and below.
		100 megohms ±1% on 500mv range and above.
VTVM, MIL-M-9996 Type I	Dc volts range:	1mv to 1000 volts in 13 ranges.
	Input resistance: (dc volts)	From 10 megohms at 1mv to 200 megohms at 300mv and above.
	Dc current range:	1ma to 1 ampere in 13 ranges.
	Accuracy:	±2 percent of full scale.

Table 6-l. Maintenance Support Equipment (cont)

EQUIPMENT IDENTIFICATION	CHARACTERISTICS	
Oscilloscope, Taktronix Model 547 with type 1A4 Plug-In	Band width:	DC to 5O MHz at 3dB
	Rise time:	7 nsec
	Sweep:	0.1 usec/cm to 5 sec/cm in 24 calibrated steps
	Vertical deflection:	10mv/cm to 20 volts/cm in 11 calibrated steps
PC Card Extender, Lockheed Part No. 7970	110 pin Processor PC card extender provides easy access to components on PC card being checked.	
SSGP Tape, STELMA Part No. 25000002-000	Provides operating program used in conjunction with Switch Interface Tester.	
PC Card Extender, STELMA Part No. 80331730-000	110-pin Processor PC card equipped with cable and female connector to facilitate interconnection of PC cards AlA3A15 through AlA3A19 under test.	
PC Card Extractor: Lockheed Part No. 7971	Plastic handle provided with two metal fingers spaced 5-12/16 inches apart enables removal of PC cards from Processor nest.	
Switch Interface Tester, STELMA Part No. 90331059-000	Provides automatic stimulus-response capability for testing RMR, RSJ, and CCL functions.	
IC Test Clip, Pomona Electronics Part No. 3916	Provides access to pins of dual in-line IC chips for test probe connections.	
PC Card Extractor Data Products Part No. 713183-l	Plastic handle provided with two spring-loaded metal fingers spaced 5-15/16 inches apart enables removal of MIA and MIB PC cards from Core Memory nest.	
PC Card Extender Data Products Part No. 715092-l	140 pin card extender provides easy access to components on Core Memory MIA and MIB PC cards being checked.	
PC Card Extender Data Products Part No. 715138-1	Comprises two 140 pin card extenders fastened to two 140 pin receptacles to provide easy access to components on Core Memory BSM being checked.	
ATP Test Tape	Provides 12 test programs and one Basic Operating System (BOS) program which checks Processor and Core Memory functions (except for Parallel I/G and I/G Controller). BOS program enables dump of Core Memory onto mag tape prior to loading of test programs.	

Table 6-l. Maintenance Support Equipment (cont)

EQUIPMENT IDENTIFICATION	CHARACTERISTICS
PC Card Extender STELMA Part No. 80331740-000	Card extender equipped with one cable and two plugs (one on each end of the cable); provides electrical connections between PC card being extended and Processor.

6-13. PROCESSOR AND CORE MEMORY PERFORMANCE TEST TABLES (EXCLUDING AUTOLOAD, PARALLEL I/O, MODEM CONTROLLER, AND I/O CONTROLLER). Before start of performance tests detailed in tables 6-2 through 6-8, check that all power switches in Data Processing Assembly A1 and TTY (KSR-35 at ACOC Group, ASR-35 at Switch Group) are ON. All tests are contained on one ATP test tape as described in paragraph 6-12. Listed below are the Processor and Core Memory tests and the applicable performance test table reference. To execute any particular performance test table, autoload the ATP test tape as described in paragraph 6-15, then follow the specific instructions given in that performance test table. Once the test(s) is completed perform the procedures of paragraph 6-16 to restore the Cm-e Memory program.

Performance Test	Test Table Reference
CPA, CPB, BUS Controller	6-2
CPA, CPB, Bus Controller Interrupt	6-3
Core Memory, Core Memory Controller	6-4
CPA, CPB, PBI, PCB, Program Maintenance Panel	6-5
Program Maintenance Panel, PBI, PCB	6-6
TTY Controller, Printer Controlle.	6-7
Mag Tape Controller, BTA	6-8

6-14. Refer to paragraphs 6-2 , through 6-31 for interpretation of error printouts resulting from faulty performance test results.

6-15. Auto-Loading ATP Test Tape.

a. Remove translucent RF1 bezel on front of Processor (AlA3) and open front panel (Program Maintenance Panel).

b. On Processor Auto Load PC card AlA3A9, set the four red toggle switches, designated from top to bottom as S1 through S4, as follows: S1 and S2 to up position, S3 and S4 to down position.

c. Mount and thread test tape on Mag Tape Unit 1 (A1A1) and a blank tape on Mag Tape Unit 2 (AlA6).

d. On both Mag Tape Units, perform the following:

1. Press LOAD switch.

2. Whera tape movement stops press LOAD switch again.

3. When LOAD lamp is lighted, press ON LINE switch.

4. If LOAD lamp is not lighted after the tape reel has made five or more revolutions, press REWIND switch; then, when LOAD lamp lights, press ON LINE switch.

e. Close the Program Maintenance Panel.

f. On the Program Maintenance Panel, press reset and then load (BOS).

g. When tape motion halts, press run.

h. TTY prints:

Table 6-2. Performance Test for CPA, CPB, and Bus Controller

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Check that all power switches in Data Processing Assy A1 and TTY, (KSR-35 at ACOC Group, ASR-35 at Switch Group) are ON.	
2			Autoload the ATP test tape per paragraph 6-15.	
3			Press reset switch then load switch.	Test tape moves forward.
4			When tape motion halts, press run switch.	Data line displays test number (hexidecimal) in bits 0 through 3. The test will loop and loop count will be displayed in bits 4 through 15.
			After observing that loop count is progressing in bits 4 through 15, repeat steps 3 and 4 three more times to complete the Performance Test for CPA, CPB, and BUS Controller.	
5			If no further testing is required press the halt switch.	

Table 6-3. Performance Test for CPA, CPB, and Bus Controller Interrupt

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Check that all power switches in Data Processing Assy A1 and TTY, (KSR-35 at ACOC Group, ASR-35 at Switch Group) are ON.	
2			Autoload the ATP test tape per paragraph 6-15.	
3			Press RESET switch then LOAD switch, five times.	Test tape moves forward.
4			When tape motion halts, press RUN switch.	TTY prints: INTERRUPT TEST REV A TST01 PRESS RUN, OPERATOR ATTENTION
5			Set LINE FREQ switch on bottom edge of Program Maintenance Panel to OFF; then, press run switch and attn switch in sequence.	No error halt. TTY prints: TST02 PRESS RUN, OPERATOR ATTENTION.
6			Press run switch and attn switch in sequence.	No error halt. TTY prints: TST03 PRESS RUN, OPERATOR ATTENTION.

Table 6-3. Performance Test for CPA, CPB, and Bus Controller Interrupt (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
7			Press run switch and attn switch in sequence.	TTY prints: TST 04 PRESS RUN, OPERATOR ATTENTION.
8			Press run switch and attn switch in sequence.	TTY prints: TST 06 DEVICE ADDR.FORMAT OUTPUT MODE = FXX1 INPUT MODE = FXX0 NO DEVICE = 0 LEVEL 2 DEVICE ADDR. =
9			Type in: F800(C/R)	TTY prints: INPUT MODE PRESS C/R
10			Press carriage return.	No error halt. TTY prints: TST 07 INPUT MODE PPESS C/R
11			Press carriage return.	No error halt. TTY prints: TST 08 INPUT MODE PRESS C/R
12			Press carriage return.	No error halt. TTY prints: TST 09 INPUT MODE PRESS C/R

Table 6-3. Performance Test for CPA, CPB, and Bus Controller Interrupt (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
13			Press carriage return.	No error halt. TTY prints: TST 10 DEVICE ADDR. FORMAT: OUTPUT MODE = FXX1 INPUT MODE = FXX0 NO DEVICE = 0 LEVEL 3 DEVICE ADDR. =
14			Type in: 0(C/R)	No error halt. TTY prints: TST 14 TURN ON LINE FREQ. CLOCK, PRESS ATTN.
15			Set LINE FREQ switch on bottom edge of Program Maintenance Panel to ON; then, press attn switch.	No error halt. TTY prints: TST 15 TST 16 TST 17 TURN OFF LINE FREQ. CLOCK, PRESS RUN.
16			Set LINE FREQ switch to OFF; then, press run switch.	No error halt. TTY prints: TST 18 1110 CPU Processor halts.

Table 6-4 Performance Test for Core Memory and Core Memory Controller

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Check that all power switches in Data Processing Assy A1 and TTY, (KSR-35 at ACOC Group or ASR-35 at Switch Group) are ON.	
2			Autoload the ATP test tape per paragraph 6-15.	
3			Press reset switch then load switch, six times.	Test tape will move forward.
4			At ACOC Group, when tape motion halts, press switches 15 and 14 in data line and switch 2 in register line. Press write switch in register line. At Switch Group, press switches 15, 14, and 13 in data line and switch 2 in register line. Press write switch in register line.	
5			Press RUN switch.	Data line will display test number in lamps 0 through 3 and loop counting in lamps 4 through 15.
6			Press halt switch; then, press clear switches in data and address lines. NOTE At Switch Group only, complete steps 7 through 11.	

Table 6-4. Performance Test for Core Memory and Core Memory Controller (cont)

OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		Press switch 0 in data line and all switches in address line to ON.	
		Press write switch in address line.	
		Press switch 9 in data line and switch 0 in register line.	
		Press write switch in register line.	
		Press run switch.	Data line will display loop counting in lamps 4 through 15.
		Press reset switch then load switch.	Test tape will move forward.
		Repeat steps 4 through 6 at ACOC Group and steps 4 through 11 at Switch Group.	Same as step 5 at ACOC Group. Same as steps 5 and 11 at Switch Group.
		Repeat steps 12 and 13.	

Table 6-5. Performance Test for CPA, CPB, PBI, PCR and Program Maintenance Panel

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Check that all power switches in Data Processing Assy A1 and TTY, (KSR-35 at ACOC Group, ASR-35 at Switch Group) are ON.	
2			Autoload the ATP test tape per paragraph 6-15.	
3			Press reset switch, then load switch, nine times.	Test tape moves forward.
4			When tape motion halts, press RUN switch.	No error halt. TTY prints: LF CLOCK/PWR FAIL TP TURN ON LF CLOCK, PWR FAIL, PWR RESTART, PRESS RUN, ATTN
5			Set the switches, located at the bottom inside edge of program maintenance panel, as follows: 1. LINE FFEQ to ON 2. PWR RC..Y to IN 3. PWR FAIL to ON	
6			Press run and attn switches.	No error halt. After approximately 30 seconds TTY prints: TST 01 CLOCK COUNT =

Table 6-5. Performance Test for CPA, CPB, PBI, PCB and Program Maintenance Panel (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
				abcd (where abcd is number of interrupts that occurred) TTY prints: TST 02 TURN POWER OFF/ON, PRESS ATTN
7			Turn OFF, and the ON, AC POWER switch on Multiple Power Supply 1, located below the Processor. Depress POWER FAIL RESET on alarm and control panel.	
8			Press ATTN switch.	No error halt. TTY prints: TST 03 TURN POWER OFF/ON, PRESS ATTN
9			Repeat steps 7 and 8.	No error halt, TTY prints: TST 04 TURN POWER OFF/ON, PRESS ATTN
10			Repeat steps 7 and 8.	Program halts.

Table 6-6. Performance Test for Program Maintenance Panel, PBI and PCB

OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		Check that all power switches in Data Processing Assy A1 and TTY; (KSR-35 at ACOC Group, ASR-35 at Switch Group) are ON; and autoload the ATP test tape per paragraph 6-15.	
		Press reset switch then load switch ten times.	Test tape moves forward.
		When tape motion halts, press RUN switch.	No error halt. TTY prints: CONTROL PANEL TP PANEL TYPE =
		Type in: 2220(C/R)	TTY prints: PANEL ADDR =
		Type in: FF80(C/R)	No error halt. TTY prints: TST 01 PRESS RESET, ATTN
		Press reset switch and then attn switch.	No error halt. TTY prints: TST 02 IF IDLE, PRESS RESET, ATTN (ERROR NOT IDLE)
		Press reset switch and then attn switch.	No error halt. TTY prints: TST 03 **DO THIS **CHECK LITES**

Table 6-6. Performance Test for Program Maintenance Panel, PBI and PCB (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
				PRESS ON OFF INH IDLE, INH ATTN IDLE, INH, ATTN ATTN IDLE, INH ATTN HALT HALT, INH INH HALT INH RUN, ATTN
8			Perform each action listed under "DO THIS" and check that lamps listed under ON are lighted and those listed under OFF are not lighted. NOTE Test 04 does not apply, since it is not implemented in this system.	No error halts. TTY prints: TST 04 TURN POWER ON/OFF KEY STRAIGHT UP VERIFY ALL SWITCHES ON PANEL ARE LOCKED OUT TURN POWER ON/OFF KEY TO RIGHT, PRESS ATTN

Table 6-6. Performance Test for Program Maintenance Panel, PBI and PCB (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
9			Press attn switch.	TTY prints: TST 05 VERIFY DATA ENTERED INTO ADDRESS/ENTRY REG = DATA/RESPONSE REG PRESS ATTN TO EXIT TEST
10			Press switches 15, 13, 11, 9, 7, 5, 3, and 1 in address line and press write switch in address line. Press read switch in address line.	No error halt. Switches 15, 13, 11, 9, 7, 5, 3, and 1 are lighted in the data line.
11			Press attn switch.	TTY prints: TST 06 AT HALT, VERIFY FOLLOWING R1=1111 R2 = 2222 R3 = 3333 R4 = 4444 R5 = 5555 R6 = 6666 R7 = 7777, PRESS RUN
12			Press switch 1 and then the read switch in register line.	No error halt. Hexidecimal 1111 is displayed in DATA line.
13			Repeat step 12 six times using switches 2, 3, 4, 5, 6, and then 7 instead of switch 1.	No error halt. Hexidecimal 2222, 3333, 4444, 5555, 6666, and 7777 are displayed in sequence, in data line.

Table 6-6. Performance Test for Program Maintenance Panel, PBI and PCB (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
14			Press run switch.	No error halt. TTY prints: TST 07 PRESS ADH, ATTN AT ADDRESS HALT VERIFY PC=abcd+-2, PRESS RESET, ATTN (where abcd is a hex number; note number)
15			Press adh and then attn switches.	
16			Press switch 0 in register line.	
17			Press read switch in register line.	No error halt. Data line display is same as abcd + or -2 of step 14.
18			Press reset and then attn switches.	
19			Repeat steps 14 through 17 two more times; the program will supply different values for abcd.	TTY prints: PRESS STEP SWITCH THREE TIMES VERIFY PC = abcd PRESS RUN (where abcd is a hex number)
20			Press step switch three times; then, press switch 0 in register line.	
21			Press read switch in register line.	Data line display is same as abcd, + or -2, of PC in step 19.

Table 6-6. Performance Test For Program Maintenance Panel, PBI and PCB (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
22			Press run switch.	No error halt. TTY prints: TST 08 STORE RANDOM DATA IN ADDRESS > abcd PRESS ATTN (where abcd is a hex number)
23			Assume abcd = F800 store 1357 in F804 as follows: Press switches 12, 9, 8, 6, 4, 2, 1, and 0 in data line. Press switches 15 through 11 and 2 in address line. Press write switch in address line; then, press write switch in register line.	
24			Press attn switch.	No error halt. TTY prints: TST 09 Shifting patterns of 1s are displayed in ADDRESS line and in DATA line. After checking each pattern the program halts.

Table 6-7. Performance Test For TTY Controller and Printer Controller

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Check that all power switches in Data Processing Assy A1 and TTY (KSR-35 at ACOC Group, ASR-35 at Switch Group) are ON. Autoload the ATP test tape per paragraph 6-15.	
2			Press reset switch then load switch, eleven times.	Test tape moves forward.
3			When tape motion halts, press RUN switch.	No error halt. TTY prints: TTY TEST TTY LEV =
4			Type in: 2(C/R)	No error halt TTY prints: TTY ADD=
5			Type in: F800(C/R) to test ASR or KSR F810(C/R) to test RO	No error halt. TTY prints: BTA=(YES=1, NO=0)
6			Type in: 0(C/R)	TTY prints: TST 01 TST 02 THE QUICK BROWN FOX SLYLY JUMPED OVER THE LAZY DOG. TST 03 !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]↑← "#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]↑← ! #$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]↑← !" $%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]↑← !"# %&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]↑← !"#$ TST A5 TYPE ON KEYBOARD

Table 6-7. Performance Test for TTY Controller and Printer Controller (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
				NOTE If RO is being tested, lines 1, 2, 4, 10, and 11 are printed on KSR. This concludes test for RO.
7			For ASR or KSR, type in several printable characters.	Character selected is printed twice.

Table 6-8. Performance Test for Mag Tape Controller and BTA

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Check that all power switches in Data Processing Assy A1 and TTY, (KSR-35 at ACOC Group, ASR-35 at Switch Group) are ON. Autoload the ATP test tape per paragraph 6-15.	
2			Press reset then load switches, twelve times.	
3			When tape motion halts press ON LINE switch to OFF.	
4			Press REWIND switch. Tape rewinds and halts. Press REWIND switch again to complete the rewind sequence. Remove test tape.	
5			Mount a blank tape (with write-enable ring) on each Mag Tape Unit. Thread the tapes, following instructions on front panel of tape transports.	
6			On both Mag Tape Units, press LOAD switch twice. When tape motion stops press ON LINE switch.	
7			Press run switch.	TTY prints: SUE MAG TAPE (BTA) TP R/R OR C (1 OR 0)=
8			Type in: 1(C/R)	TTY prints: ADDR =

Table 6-8. Performance Test for Mag Tape Controller and BTA (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
9			Type in: F8C0(C/R)	TTY prints: LVL =
10			Type in: 3(C/R)	TTY prints: # DRIVES =
11			Type in: 2(C/R)	TTY prints: RD/WRT OR WRT (1 OR 0) =
12			Type in: 1(C/R)	TTY prints: SET DRV SLCT UNIT 0=0, UNIT 1=1, ETC, PRS RUN
13			Press run switch.	No error halt. TTY prints: DFN TST PRMTRS (1 OR 0) =
14			Type in: 0(C/R)	TTY prints: RCDS=
15			Type in: 20(C/R)	TTY prints: WRDS=
16			Type in: 5(C/R)	TTY prints: DATA =
17			Type in: A55A(C/R)	TTY prints: RWND & LV ALL UNITS ON LINE, LOAD, WRT EN, PRS RUN

Table 6-8 Performance Test for Mag Tape Controller and BTA (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
18			Press run switch.	No error halt. TTY prints: TST 01 ** UNIT 0 ** UNIT 1 ** UNIT 0 TST 02 TST 03 TST 04 TST 05 TST 06 TST 07 TST 08 TST 09 TST 10 TST 11 ** UNIT 1 TST 02 TST 03 TST 04 TST 05 TST 06 TST 07 TST 08 TST 09 TST 10 TST 11 END OF TEST LP CT=0001 ** UNIT 0 TST 02 TST 03 TST 04 TST 05

Table 6-8. Performance Test for Mag Tape Controller and BTA (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
				TST 06 TST 07 TST 08 TST 09 TST 10 TST 11 ** UNIT 1 TST 02 TST 03 TST 04 TST 05 TST 06 TST 07 TST 08 TST 09 TST 10 TST 11 END OF TEST LP CT=0002
19			Press halt switch.	

i. Type in:
ASSIGN BOE (C/R)

j. TTY prints: >

At the Switch Group, type in:
DUMP, 0, IDFFF, XXXX(CR)

NOTE: This should be a valid start address for SSP.

At the ACOC Group, type in:
DUMP, 0., 7FFF, XXXX(CR)

NOTE: This should be a valid start address for SSP.

k. Tape unit A6 will move forward recording information from core area specified in step j.

1. When tape unit A6 stops TTY prints > . Depress ON LINE switch to OFF and depress REWIND switch. Depress REWIND switch once more to complete the rewind sequence.

m. Remove the tape from unit A6 and save. This is a program dump from Core Memory used to restore the Core Memory at completion of the Processor and Core Memory performance tests (refer to paragraph 6-16).

6-16. Restoring Core Memory. After performing required performance test(s), restore Core Memory program dumped onto tape in paragraph 6-15, as follows:

a. Place the tape, containing core memory information, onto Mag Tape Unit Al. Thread this tape, following instructions on front panel of tape transport.

b. Depress LOAD switch. When tape motion halts, depress LOAD switch once more.

C. When tape motion halts, LOAD indicator lights.

d. Depress ON LINE switch to ON,

e. On Program Maintenance Panel, press reset switch and then load switch.

f. When tape motion halts, press run switch.

g- Tape will move forward loading its contents back into core memory.

6-17. AUTOLOAD PERFORMANCE TEST. There are no performance test tables specifically for the autoload function of the Processor. If the autoload function can be accomplished as described in paragraph 6-15, then the autoload function meets minimum performance standards.

6-18. PARALLEL I/O PERFORMANCE TEST. There are no performance test tables specifically for the Parallel I/O. To determine if the Parallel I/O is functioning properly, perform the PFD/Clock, Alarm Control, and VF Communication Link tests in Section III, Chapter 6 of the appropriate group technical manual (T.O. 31W2-2G-271 for the Switch Group, T.O. 31W2-2G-281 for the ACOC Group).

6-19. MODEM CONTROLLER PERFORMANCE TEST. There are no performance test tables specifically for the Modem Controller. To determine if the Modem Controller is functioning properly, perform the VF Communications Link test in Section III, Chapter 6 of the appropriate group technical manual (T.O. 31W2-2G-271 for the Switch Group: T.O. 31W2-2G-281 for the ACOC Group).

6-20. I/O CONTROLLER (SWITCH GROUP ONLY) PERFORMANCE TEST. There are no performance test tables specifically for the I/O Controller. To determine if the I/O Controller is functioning properly, perform the RMR, RSJ, and CCL tests in Section III, Chapter 6 of T.O. 31W2-2G-271.

6-21. VOLTAGE REQUIREMENTS AND SOURCES.

6-22. All dc voltage requirements for the Processor and Core Memory are provided by Multiple Power Supplies 1 and 2. The dc operating voltages required by the various PC cards are listed in Table 6-9.

6-23. ALIGNMENT.

6-24. Adjustment procedures for the CM MSA 2.75 volt dc power supply should be performed on each CM MSA PC card. The Switch Group contains four BSM's and the ACOC Group contains three BSM's each of which includes a CM MSA PC card. Each

Table 6-9. DC Voltage Requirements and Sources

COMPONENT	DC OPERATING VOLTAGES	VOLTAGE SOURCES
Processor A3	5 volts	Multiple Power Supply (A1A5): TB1-1 TB1-2 TB1-3 TB1-4 TB1-5
	15 volts	TB3-1
	-15 volts	TB3-5 TB3-6
Bus Controller A5	5 volts	Processor (A1A3): XA6-A16 XA6-B16 XA6-A28 XA6-B28 XA6-A29 XA6-B29 XA6-A51 XA6-B51
CPA A6	5 volts	Processor (A1A3): XA6-A16 XA6-B16 XA6-A28 XA6-B28 XA6-A29 XA6-B29 XA6-A51 XA6-B51
CPB A7	5 volts	Processor (A1A3): XA7-A16 XA7-B16 XA7-A28 XA7-B28 XA7-A29 XA7-B29 XA7-A51 XA7-B51
	15 volts	XA7-A52 XA7-B52 XA7-A53 XA7-B53

Table 6-9. DC Voltage Requirements and Sources (cont)

COMPONENT	DC OPERATING VOLTAGES	VOLTAGE SOURCES
Core Memory Controller A8	5 volts	Processor (A1A3): XA8-A16 XA8-A28 XA8-A29 XA8-A51
Autoload A9	5 volts	Processor (A1A3): XA9-A16 XA9-B16 XA9-A28 XA9-B28 XA9-A29 XA9-B29 XA9-A51 XA9-B51
Parallel I/O A10	5 volts	Processor (A1A3): XA10-A16 XA10-B16 XA10-A28 XA10-B28 XA10-A29 XA10-B29 XA10-A51 XA10-B51
TTY Controller A11	5 volts	Processor (A1A3): XA11-A16 XA11-B16 XA11-A28 XA11-B28 XA11-A29 XA11-B29 XA11-A51 XA11-B51
	15 volts	XA11-A3 XA11-B3 XA11-A4 XA11-B4
	-15 volts	XA11-A52 XA11-B52 XA11-A53 XA11-B53

Table 6-9. DC Voltage Requirements and Sources (cont)

COMPONENT	DC OPERATING VOLTAGES	VOLTAGE SOURCES
Modem Controller 1 A12	5 volts	Processor (A1A3): XA12-A16 XA12-B16 XA12-A28 XA12-B28 XA12-A29 XA12-B29 XA12-A51 XA12-B51
	15 volts	XA12-A3 XA12-B3 XA12-A4 XA12-B4
	-15 volts	XA12-A52 XA12-B52 XA12-A53 XA12-B53
Block Transfer Adapter A13	5 volts	Processor (A1A3): XA13-A16 XA13-B16 XA13-A28 XA13-B28 XA13-A29 XA13-B29 XA13-A51 XA13-B51
Mag Tape Controller A14	5 volts	Processor (A1A3): XA14-A16 XA14-B16 XA14-A28 XA14-B28 XA14-A29 XA14-B29 XA14-A51 XA14-B51

Table 6-9. DC Voltage Requirements and Sources (cont)

COMPONENT	DC OPERATING VOLTAGES	VOLTAGE SOURCES
I/O Controller A15 (Switch Group)	5 volts	Processor (A1A3): XA15-A16 XA15-B16 XA15-A28 XA15-B28 XA15-A29 XA15-B29 XA15-A51 XA15-B51
Printer Controller A15 (ACOC Group)	5 volts	Processor (A1A3): XA15-A16 XA15-B16 XA15-A28 XA15-B28 XA15-A29 XA15-B29 XA15-A51 XA15-B51
	15 volts	XA15-A3 XA15-B3 XA15-A4 XA15-B4
	-15 volts	XA15-A52 XA15-B52 XA15-A53 XA15-B53
Modem Controller 2 A16 (ACOC Group)	5 volts	Processor (A1A3): XA16-A16 XA16-B16 XA16-A28 XA16-B28 XA16-A29 XA16-B29 XA16-A51 XA16-B51
	15 volts	XA16-A3 XA16-B3 XA16-A4 XA16-B4

Table 6-9. DC Voltage Requirements and Sources (cont)

COMPONENT	DC OPERATING VOLTAGES	VOLTAGE SOURCES
	-15 volts	XA16-A52 XA16-B52 XA16-A53 XA16-B53
PBI A17 (ACOC Group); A20 (Switch Group)	5 volts	Processor (A1A3): XA17;20-A16 XA17;20-B16 XA17;20-A28 XA17;20-B28 XA17;20-A29 XA17;20-B29 XA17;20-A51 XA17;20-B51
PCB A18 (ACOC Group); A21 (Switch Group)	5 volts	Processor (A1A3): XA18;21-A16 XA18;21-B16 XA18;21-A28 XA18;21-B28 XA18;21-A29 XA18;21-B29 XA18;21-A51 XA18;21-B51
Core Memory A8	5 volts	Multiple Power Supply 2 (A1A10): TB1-1 TB1-2 TB1-3
	-15 volts	TB3-5 TB3-6
CM MIA A1	5 volts	Core Memory (A1A8): XA11P1-5 XA11P1-6 XA11P1-7 XA11P1-8

Table 6-9. DC Voltage Requirements and Sources (cont)

COMPONENT	DC OPERATING VOLTAGES	VOLTAGE SOURCES
CM MIB, A2	5 volts	Core Memory (A1A8): XA10P1-5 XA10P1-6 XA10P1-7 XA10P1-8
CM MSA A3A3, A4A3 (ACOC Group); A3A3, A4A3, A5A3, A6A3 (Switch Group)	5 volts	Core Memory (A1A8): XA9A3P1, XA8A3P1 (ACOC Group); XA9A3P1, XA8A3P1, XA7A3P1, XA6A3P1 (Switch Group) P1-5 P1-6 P1-7 P1-8 P1-9 P1-10
	-15 volts	XA9A3P1, XA8A3P1, (ACOC Group); XA9A3P1, XA8A3P1, XA7A3P1, XA6A3P1 (Switch Group) P1-132 P1-133 P1-134 P1-135 P1-136
CM MBA, A3A1, A4A1 (ACOC Group); A3A1, A4A1, A5A1, A6A1 (Switch Group)	5 volts	Core Memory (A1A8): XA9A1P1, XA8A1P1 (ACOC Group) XA9A1P1, XA8A1P1, XA7A1P1, XA6A1P1 (Switch Group) P1-5 P1-6 P1-7 P1-8
	-15 volts	XA9A1P1, XA8A1P1 (ACOC Group) XA9A1P1, XA8A1P1, XA7A1P1, XA6A1P1 (Switch Group) P1-131 P1-132 P1-133 P1-134 P1-135 P1-136

CM MSA PC card contains a 2.75 volt dc power supply which supplies core matrix drive current. The 2.75 volt power supply adjustment is described below.

a. With system power turned off, remove BSM and place on extenders.

b. Turn on system power.

c. Connect dc voltmeter between Q2-C and pin Pl-1 on CM MSA and check that a measurement of 2.75 volts dc is obtained. If necessary adjust Rl for proper reading.

6-25. TEST ERROR PRINTOUTS.

6-26. When the interrupt, LF and power fail restart, control panel, teletype 33/35, or SUE Mag tape (BTA) acceptance tests are used during a performance test, standard error messages may be printed on the TTY. The following paragraphs describe these error messages. It should be noted that during performance tests that utilize GINS I through IV, memory address, random data, and worst pattern memory acceptance tests no TTY error print outs are generated.

6-27. PROCESSOR INTERRUPT TEST ERROR PRINTOUTS. If an error is detected during the Processor interrupt test, the TTY will type a standard error message in the following format:

T xx A yyyy B z

Where xx indicates the test number in which the error was detected, yyyy indicates the program address where the error occurred, and z indicates the type of error. See table 6-10 for definitions of test numbers and table 6-11 for definitions of types of errors.

Table 6-10. Processor Interrupt Test Number Definitions

TEST NUMBER	DEFINITION
01	Detect Level 1 Interrupt Test
02	Enable and Wait Level 1 Interrupt Test
03	Disable and Wait Level 1 Interrupt Test
04	Wait for Interrupt Level 1 Test
06	Detect Level 2 Interrupt Test
07	Enable and Wait Level 2 Interrupt Test
08	Disable and Wait Level 2 Interrupt Test
09	Wait for Interrupt Level 2 Test
10	Detect Level 3 Interrupt Test
11	Enable and Wait Level Three Interrupt Test
12	Disable and Wait Level 3 Interrupt Test
13	Wait for Interrupt Level 3 Test

Table 6-10. Processor Interrupt Test Number Definitions (cont)

TEST NUMBER	DEFINITION
14	Detect Level 4 Interrupt Test
15	Enable and Wait Level 4 Interrupt Test
16	Disable and Wait Level 4 Interrupt Test
17	Wait for Interrupt Level 4 Test
18	Unimplemented Instruction Interrupt (Level 5) Interrupt Test
19	Abort (Level 6) Interrupt Test Using JUMP Instruction
20	Abort (Level 6) Interrupt Test Using MOVW Instruction
21	Abort (Level 6) Interrupt Test Using ANDW Instruction
22	Abort (Level 6) Interrupt Test Using SUBW Instruction

Table 6-11. Processor Interrupt Test Error Definitions

TYPE OF ERROR	DEFINITION
0	Status Error
1	Data Error
2	Timing Error
3	No Interrupt
4	Device Address Error
5	Undefined
6	Undefined
7	Undefined

Table 6-11. Processor Interrupt Test Error Definitions (cont)

TYPE OF ERROR	DEFINITION
8	Non-continuous Execution
9	Interrupt Code Error
A	Program Counter Error

6-28. LF CLOCK AND POWER FAIL TEST ERROR PRINTOUTS. If an error is detected during the LF Clock and power fail test, the TTY will type a standard error message in the following format:

T xx A yyyy B z

Where xx indicates the test number in which the error was detected, yyyy indicates the program address where the error occurred, and z indicates the type of error. See table 6-12 for definitions of test numbers and table 6-13 for definitions of types of errors.

Table 6-12. LF Clock and Power Fail Test Number Definitions

TEST NUMBER	DEFINITION
01	Line Frequency Clock Test
02	Power Fail/Restart Load Core Memory with FFFF 16 Test
03	Power Fail/Restart Load Core Memory with 0000 16 Test
04	Power Fail/Restart Clear Core Memory Test

Table 6-13. LF Clock and Power Fail Test Error Definitions

TYPE OF ERROR	DEFINITION
0	Status Error
1	Data Error
2	Timing Error
3	No Interrupt

Table 6-13. LF Clock and Power Fail Test Error Definitions (cont)

TYPE OF ERROR	DEFINITION
4	Device Address Error
5	Undefined
6	Undefined
7	Undefined
8	Error CPU Clock Out of Specification
9	Error Test Out of Sequence
A	Error PF Net Equal to Restart
B	Error Power Fail Delay Not Long Enough
C	Error PC Wrong Value

6-29. PROGRAM MAINTENANCE PANEL TEST ERROR PRINTOUTS. If an error is detected during the Program Maintenance Panel test, the TTY will type a standard error message in the following format:

T xx A yyyy B z

Where xx indicates the test number in which the error was detected, yyyy indicates the program address where the error occurred, and z indicates the type of error. See table 6-14 for definitions of test numbers and table 6-l5 for definitions of types of errors.

Table 6-14. Program Maintenance Panel Test Number Definitions

TEST NUMBER	DEFINITION
01	Reset and attn Test
02	Idle Test
03	Inh, Att, and Halt Lamps and Switches Test
04	Keylock Switch Test
05	Read and Display Data Test
06	Load Data Test

Table 6-14. Program Maintenance Panel Test Number Definitions (cont)

TEST NUMBER	DEFINITION
07	Address Halt Test
08	Write Data Test
09	Write and Read Address Register Test

Table 6-15. Program Maintenance Panel Test Error Definitions

TYPE OF ERROR	DEFINITION
0	Status Error
1	Data Error
2	Timing Error
3	No Interrupt
4	Device Address Error
5	Undefined
6	Undefined
7	Undefined
8	Address Halt Error
9	Error Interrupt Occurred
A	Error Address Register

6-30. TTY TEST ERROR PRINTOUTS. If an error is detected during the TTY test, the TTY will type a standard error message in the following format:

T xx A yyyy B z

Where xx indicates the test number in which the error was detected, yyyy indicates the program address where the error occurred, and z indicates the type of error. See table 6-16 for definitions of test numbers and table 6-17 for definitions of types of errors.

Table 6-16. TTY Test Number Definitions

TEST NUMBER	DEFINITION
01	I/O Status Register and I/O Control Register Tests
02	Data Output, PDT Status Bit, and Data Transmission Test
03	ASCII Character test
A3	Input and Output Character Test
04	ASCII Character Status Test
05	ASCII Character Read Test
06	TTY Punched Tape PDT Test
07	TTY Punched Tape BTA Test

Table 6-17. TTY Test Error Definitions

TYPE OF ERROR	DEFINITION
0	**Status** Error
1	Data Error
2	Timing Error
3	No Interrupt
4	Device Address Error
5	Undefined
6	Undefined
7	Undefined
8	Block Length Register or I/O Buffer Address Error
9	I/O Control Register Error
A	End of Record Stop Error
B	Status Error at Interrupt Level

6-31. MAG TAPE CONTROLLER (BTA) TEST ERROR PRINTOUTS. If an error is detected during the Mag Tape Controller (BTA) test, the TTY will type a standard error message in the following format:

T xx A yyyy B z

Where xx indicates the test number in which the error was detected, yyyy indicates the program address where the error occurred, and z indicates the type of error. See table 6-18 for definitions of test numbers and table 6-19 for definitions of types of errors.

Table 6-18. Mag Tape Controller (BTA) Test Number Definitions

TEST NUMBER	DEFINITION
01	Manual Test
02	Basic Motion Test
03	Basic Write with Enable Interrupt Test
04	Basic Read with Enable Interrupt Test
05	Transfer Timing Test
06	No Data Encountered Test
07	Command Acceptance Test
08	Write with Enable Interrupt Test
09	Read with Enable Interrupt Test
10	Performance Test
11	Formatter Interrupt Test

Table 6-19. Mag Tape Controller (BTA) Test Error Definitions

TYPE OF ERROR	DEFINITION
	Controller Status Error
	Data Error (CRC, LRD)
	Timing Error
	No BTA Completion Interrupt
	Device Address Error

Table 6-19. Mag Tape Controller (BTA) Test Error Definitions (cont)

TYPE OF ERROR	DEFINITION
5	Formatter Status Error
6	No Tape Stop Interrupt
7	No Data Encountered Error
8	BTA Abort
9	BTA Block Length/End Address Error
A	No formatter Interrupt When Conditions Met
B	Undefined
C	No PDT Int when Int Enabled
D	Data Transmission Error
E	PDT Bit was off
F	Undefined

SECTION II

SPECIAL MAINTENANCE

6-32. GENERAL.

6-33. The special maintenance procedures described in the following paragraphs are performed on an off-line basis with the PC card connected to the system via the appropriate card extender; therefore, no special bench-test setups are required. Maintenance procedures are provided in the form of component performance test tables.

6-34. COMPONENT PARTS IDENTIFICATION.

6-35. Parts identification illustrations for components not identified on the equipment are provided in separate Circuit Diagrams manual. Refer to separate Circuit Diagrams manual for component, equipment, and interconnecting schematic diagrams.

6-36. COMPONENT PERFORMANCE TEST TABLES.

6-37. The component performance test tables contain information that, if used as directed, will isolate PC card malfunctions to an integrated circuit (IC) or group of ICs. During the tests, reference should be made to the appropriate schematic diagrams in T.O. 3185-4-308-3. To perform a specific test, refer to the applicable paragraph listed below and proceed as directed.

PC Card	Paragraph
Autoload	6-38
Bus Controller	6-40
CPA	6-42
CPB	6-44
Core Memory Controller	6-46
CM MlA	6-48
CM MlB	6-50
CM MSA	6-52
CM MBA	6-54
CM MMA	6-56
PCB	6-58
PBI	6-60
TTY Controller	6-62
Mag Tape Controller	6-64
Block Transfer Adapter	6-66
I/O Controller	6-68
Parallel I/O	6-70
Modem Controller 1	6-71
Printer Controller	6-73
Modem Controller 2	6-75

NOTE

The test procedures make extensive use of waveform observation. Since the Processor and Core Memory operate a synchronously under program control and because of differences in environmental conditions and component tolerances, these waveforms are intended for reference only. The actual length (or the interval between) monitored waveforms may vary greatly from those provided as references. In addition waveforms observed on the Processor INFIBUS contain extraneous data; however, the test procedure indicates only the portion of the waveform that is pertinent to the test. Therefore, repetivity patterns and over-all shape, rather than timing should be the major factors in determining whether any waveform is correct.

6-38. AUTOLOAD PC CARD COMPONENT PERFORMANCE TEST. The component performance test for the Autoload PC card is used to isolate malfunctions to an IC or group of IC's. **To** accomplish the Autoload PC **card component** performance test, per**form the** procedure in table 6-20.

6-39. After step 5 of table 6-20, load Switch Group or ACOC Group program tape as follows:

Table 6-20. Autoload PC Card A1A3A9, Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
2			Remove four screws that secure bezel to front of Processor.	
3			Open Program Maintenance Panel SWB.	
4			Place Autoload PC card A1A3A9 on card extender.	
5			Set AC POWER 120V switch on Multiple Power Supply 1 to ON and press POWER ALARM RESET switch on Alarm and Control Panel.	
6			For instructions to load program tape see paragraph 6-39.	
7	Sequentially connect oscilloscope to test points and adjust to observe indicated waveform.	U6-12		2.4 to 5.2 VDC level
		U7-11		2.4 to 5.2 VDC level

Table 6-20. Autoload PC Card AlA3A9, Performance Test (cont)

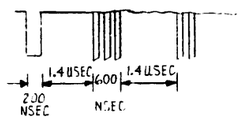
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U51-6		2.4 to 5.2 VDC level
		U61-9		0 VDC
		U55-6		
		U47-8		Same as U55-6

Table 6-20. Autoload PC Card AlA3A9, Performance Test (cont)

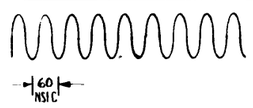
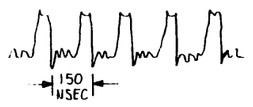
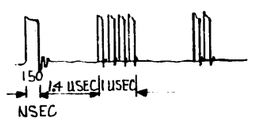
OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
	U77-6		
	U77-3		
	U65-14		
	U65-13		Same as U65-14

Table 6-20. Autoload PC Card A1A3A9, Performance Test (cont)

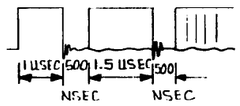
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U65-11		Same as U65-14
		U65-10		Same as U65-14
		U35-9		
		U21-3		2.4 to 5.2 VDC

Table 6-20. Autoload PC Card A1A3A9, Performance Test (cont)

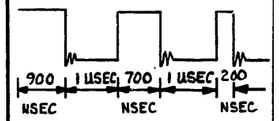
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U21-8		2.4 to 5.2 VDC
		U21-11		2.4 to 5.2 VDC
		U21-6		
		U33-8		2.4 to 5.2 VDC

Table 6-20. Autoload PC Card A1A3A9, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U53-11		0 VDC
		U63-8		0 VDC
		U73-8		0 VDC
		U74-12		2.4 to 5.2 VDC level

Table 6-20. Autoload PC Card A1A3A9, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U54-8		2.4 to 5.2 VDC level
		U64-6		2.4 to 5.2 VDC level
		U63-6		2.4 to 5.2 VDC level
		U52-6		0 VDC

Table 6-20. Autoload PC Card A1A3A9, Performance Test (cont)

OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
	U6-8		2.4 to 5.2 VDC level
	U12-8		2.4 to 5.2 VDC level
	U34-8		2.4 to 5.2 VDC level
	U3-11		0 VDC

Table 6-20. Autoload PC Card A1A3A9, Performance Test (cont)

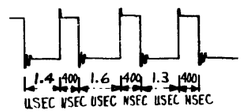
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U14-3		2.4 to 5.2 VDC level
		U23-6		2.4 to 5.2 VDC level
		U53-6		2.4 to 5.2 VDC level
		U7-3		

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Table 6-20. Autoload PC Card A1A3A9. Performance Test (cont)

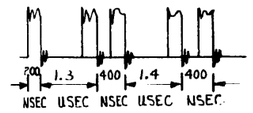
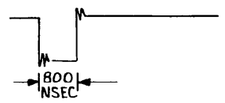
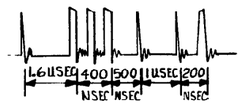
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U7-6		
		U36-10		
		U66-8		
		U66-6		Same as U66-8

Table 6-20. Autoload PC Card AlA3A9, Performance Test (cont)

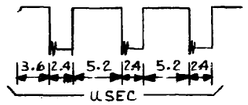
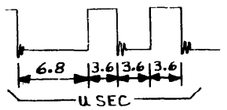
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U56-8		Same as U66-8
		U46-6		Same as U66-8
		U69-7		
		U69-4		

Table 6-20. Autoload PC Card A1A3A9, Performance Test (cont)

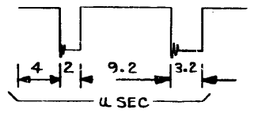
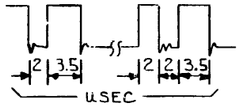
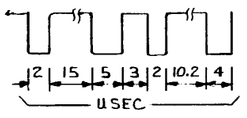
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U69-9		
		U69-10		0 VDC
		U59-7		
		U59-4		

Table 6-20. Autoload PC Card A1A3A9, Performance Test (cont)

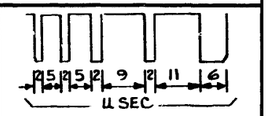
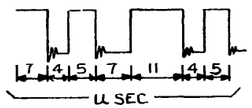
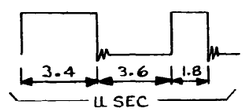
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U59-9		
		U59-12		
		U77-11		Same as U65-14
		U50-4		

Table 6-20. Autoload PC Card A1A3A9, Performance Test (cont)

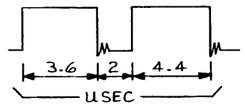
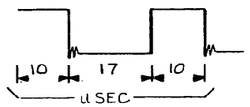
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U50-2		
		U50-13		
		U67-6		Same as U65-14
		U39-7		Same as U50-2

Table 6-20. Autoload PC Card A1A3A9, Performance Test (cont)

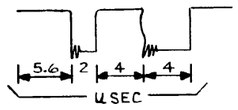
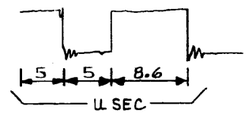
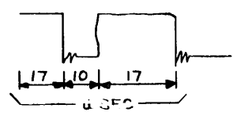
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U39-4		
		U39-9		
		U39-12		
		U67-8		Same as U65-14

Table 6-20. Autoload PC Card A1A3A9, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
8			Rewind and remove program tape.	
9			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
10			Reinstall Autoload PC Card A1A3A9 in Processor.	
11			Close Program Maintenance Panel.	
12			Secure bezel to Processor with four screws.	

a. Open Program Maintenance Panel.

b. On Processor Auto-Load PC card A1A3A9, set the four red toggle switches, designated from top to bottom as S1 through S4, as follows: S1 and S2 to up position, S3 and S4 to down position.

Mount and thread program tape on Mag 'Tape Unit 1 (AlAl).

d. On Mag Tape Unit, perform the following:

1. Press LOAD switch.

2. When tape movement stops press LOAD switch again.

3. When LOAD lamp is lighted, press ON LINE switch.

4. If LOAD lamp is not lighted after the tape reel has made five or more revolutions, press REWIND switch; then, when LOAD lamp lights, press ON LINE switch.

e. Press reset and load switches on the Program Maintenance Panel

f. When tape motion halts press run switch.

g. Proceed to step 7 of table 6-20.

h. Program tape must be loading while readings are being taken. If necessary, rewind and reload program tape, as required to continue test.

6-40. BUS CONTROLLER PC CARD COMPONENT PERFORMANCE TEST. The component performance test for the Bus Controller PC card is used to isolate malfunctions to an XC or group of IC'S. To accomplish the Bus Controller PC card component performance test perform the procedure in table 6-21.

6-41. After step 7 of table 6-21, load the ATP tape as follows:

a. Open Program Maintenance Panel.

b. On Processor Auto-Load PC card A1A3A9, set the four red toggle switches, designated from top to bottom as Sl through S4, as follows: Sl and S2 to up position, S3 and S4 to down position.

Mount and thread ATP tape on Mag Tape Unit 1 (AlAl).

d. On Mag Tape Unit, perform the following:

1. Press LOAD switch.

2. When tape movement stops press LOAD switch again.

3. When LOAD lamp is lighted, press ON LINE switch.

4. If LOAD lamp is not lighted after the tape reel has made five or more revolutions, press REWIND switch; then, when LOAD lamp lights, press ON LINE switch.

e. Press reset and load switches.

f. When tape motion stops, repeat step e four more times to reach the fifth program (GIN 4). Tape motion must stop after each load.

g. Press run switch after the fifth load.

NOTE

A loop count will appear in bits 4 to 14 and bit 2 will light to indicate GIN 4 is operating.

h. Go to step 9 of table 6-21.

6-42. CPA PC CARD COMPONENT PERFORMANCE TEST. The component performance test for the CPA PC card is employed to isolate malfunctions to an IC or group of IC's. To accomplish the CPA PC card component performance test perform the procedure in table 6-22.

6-43. After step 7 of table 6-22, load the ATP tape as follows:

Table 6-21. Bus Controller PC Card A1A3A5, Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
2			Remove four screws that secure bezel to Processor.	
3			Open Program Maintenance Panel.	
4			Remove Interconnect Module from PC cards A1A3A5, A1A3A6, and A1A3A7.	
5			Place Bus Controller PC card A1A3A5, CPB PC card A1A3A6, and CPA PC card A1A3A7 on card extenders.	
6			Replace Interconnect Module on front of PC cards A1A3A5, A1A3A6, and A1A3A7.	
7			Set AC POWER 120V switch on Multiple Power Supply 1 to ON. Press POWER ALARM RESET switch on Alarm and Control Panel.	
8			For instructions to load ATP tape, see paragraph 6-41.	
9	Connect frequency counter to test point and adjust to observe indicated frequency.	U78-6		25 MHz ±0.01 percent

Table 6-2 I. Bus Controller PC Card A1A3A5, Performance Test (cont) NAVELEX 0967-464-0010

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
10	Sequentially connect oscilloscope to test points and adjust to observe indicated waveform.	U14-11		2.4 to 5.2 VDC level
		U6-5		0 volts
		U8-3		2.4 to 5.2 VDC level
		U4-12		2.4 to 5.2 VDC level

Table 6-21. Bus Controller PC Card A1A3A5, Perfomance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U43-6		0 volts
		U43-4		0 volts
		U43-2		0 volts
		U43-9		0 volts

Table 6-21. Bus Controller PC Card A1A3A5, Performance Test (cont)

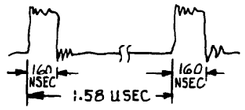
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U43-11		
		U52-2		0 volts
		U52-4		0 volts
		U52-6		0 volts

Table 6-21. Bus Controller PC Card A1A3A5, Performance Test (cont)

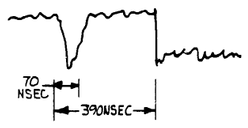
OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
	U52-9		
	U52-11		Same as U43-11
	U55-6		2.4 to 5.2 VDC level
	U71-12		

Table 6-21. Bus Controller PC Card A1A3A5, Performance Test (cont)

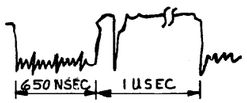
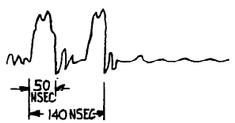
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U71-5		
		U71-13		Same as U71-5
		U71-4		
		U24-1		

Table 6-21. Bus Controller PC Card A1A3A5, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U56-8		2.4 to 5.2 VDC level
		U24-4		2.4 to 5.2 VDC level
		U63-11		0 volts
		U65-2		2.4 to 5.2 VDC level

Table 6-21. Bus Controller PC Card A1A3A5, Performance Test (cont)

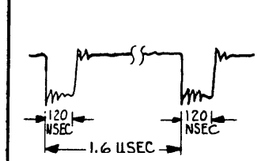
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U65-15		0 volts
		U65-7		0 volts
		U65-11		0 volts
		U34-6		

Table 6-21. Bus Controller PC Card A1A3A5, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U47-8		Reverse of U34-6
		U31-8		0 volts
		U32-8		2.4 to 5.2 VDC level
		U21-12		0 volts

Table 6-21. Bus Controller PC Card A1A3A5, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U4-8		2.4 to 5.2 VDC level
		U3-6		
		U63-3		2.4 to 5.2 VDC level
		U14-6		2.4 to 5.2 VDC level

Table 6-21. Bus Controller PC Card A1A3A5, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U76-8		2.4 to 5.2 VDC level (ON/OFF 1/sec)
		U56-6		0 volts
		U68-3		2.4 VDC level (ON/OFF 1/sec)
		U6-14		1.8 VDC

Table 6-21. Bus Controller PC Card A1A3A5, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U63-6		0 volts
		U56-3		2.4 to 5.2 VDC level
		U17-4		0 volts
		U27-8		2.4 to 5.2 VDC level

Table 6-21. Bus Controller PC Card A1A3A5, Performance Test (cont)

P	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
			Rewind and remove ATP tape. Set AC POWER 120V switch on Multiple Power Supply 1 to OFF. Disconnect Interconnect Module from PC cards A1A3A5, A1A3A6, and A1A3A7. Remove PC cards A1A3A5, A1A3A6, and A1A3A7 from card extenders; then, remove card extenders. Reinstall PC cards A1A3A5, A1A3A6, and A1A3A7 in Processor. Replace Interconnect Module on front of PC cards A1A3A5, A1A3A6, and A1A3A7. Close Program Maintenance Panel. Secure bezel to Processor with four screws.	

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Table 6-22. CPA PC Card A1A3A7, Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
2			Remove four screws that secure bezel to Processor.	
3			Open Program Maintenance Panel.	
4			Remove Interconnect Module from PC cards A1A3A5, A1A3A6, and A1A3A7.	
5			Place CPA PC card A1A3A7 and CPB PC card A1A3A6 on card extenders.	
6			Connect Interconnect Module Adapter to CPA PC card A1A3A7, CPB PC card A1A3A6 and BUS Controller PC card A1A3A5.	
7			Set AC POWER 120V switch on Multiple Power Supply 1 to ON. Press POWER ALARM RESET switch on Alarm and Control Panel.	
8			For instructions to load ATP tape see paragraph 6-43.	
9	Sequentially connect oscilloscope to test points and adjust to observe indicated waveform.	U76-8		0 VDC

Table 6-22. CPA PC Card A1A3A7, Performance Test (cont)

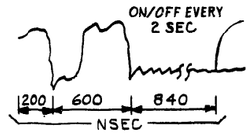
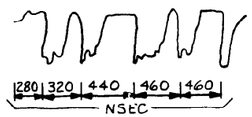
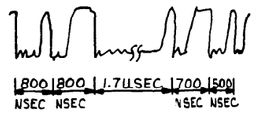
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U2-3		
		U2-6		
		U2-8		0 VDC
		U2-11		

Table 6-22. CPA PC Card A1A3A7, Performance Test (cont)

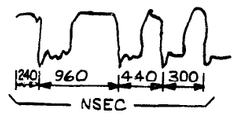
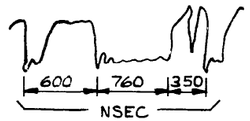
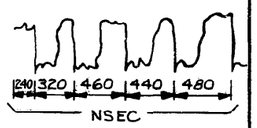
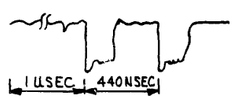
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U32-3		
		U32-6		
		U12-3		
		U32-8		

Table 6-22. CPA PC Card A1A3A7, Performance Test (cont)

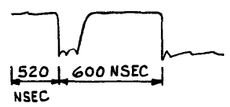
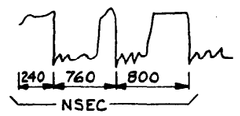
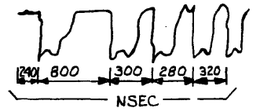
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U12-6		Same as U12-3
		U32-11		
		U12-8		
		U22-3		

Table 6-22. CPA PC Card A1A3A7, Performance Test (cont)

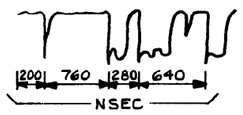
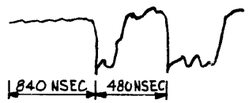
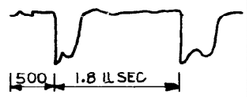
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U12-11		
		U22-6		Same as U22-3
		U22-8		
		U22-11		

Table 6-22. CPA PC Card A1A3A7, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U16-2		0 VDC
		U16-7		0 VDC
		U16-10		0 VDC
		U16-15		0 VDC

Table 6-22. CPA PC Card AlA3A7, Performance Test (cont)

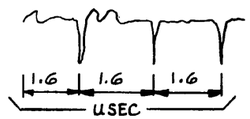
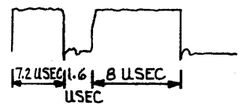
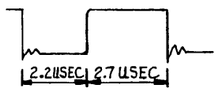
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE* STANDARDS
		U16-9		
		U6-2		0 VDC
		U26-2		
		U6-7		

Table 6-22. CPA PC Card AlA3A7, Performance Test (cont)

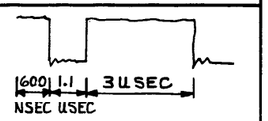
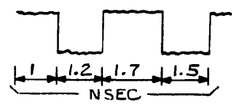
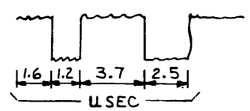
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U26-7		
		U6-10		
		U26-10		
		U6-15		0 VDC

Table 6-22. CPA PC Card AlA3A7, Performance Test (cont)

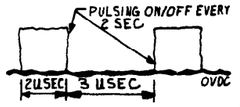
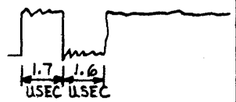
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U26-15		
		U6-9		Same as U16-9
		U36-2		
		U36-7		Same as U36-2

Table 6-22. CPA PC Card A1A3A7, Performance Test (cont)

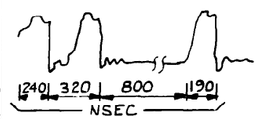
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U46-5		2.4 to 5.2 VDC level
		U46-9		2.4 to 5.2 VDC level
		U47-1		2.4 to 5.2 VDC level
		U7-7		

Table 6-22. CPA PC Card A1A3A7, Performance Test (cont)

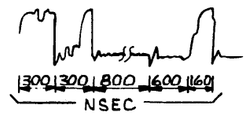
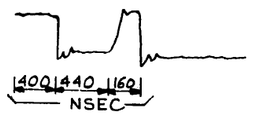
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U27-7		
		U8-7		
		U28-7		Same as U27-7
		U7-9		Same as U27-7

Table 6-22. CPA PC Card A1A3A6, Performance Test (cont)

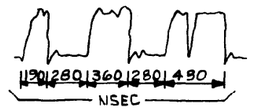
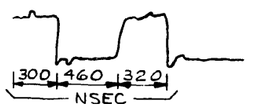
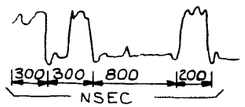
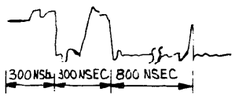
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U27-9		
		U8-9		
		U28-9		
		U17-7		

Table 6-22. CPA PC Card A1A3A7, Performance Test (cont)

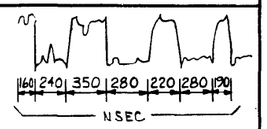
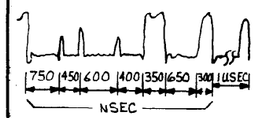
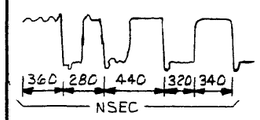
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U37-7		
		U18-7		
		U38-7		
		U17-9		Same as U17-7

Table 6-22. CPA PC Card A1A3A7, Performance Test (cont)

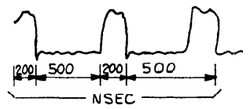
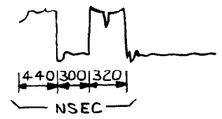
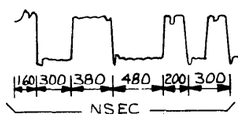
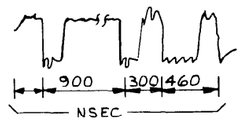
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U37-9		
		U18-9		
		U38-9		
		U48-2		

Table 6-22. CPA PC Card A1A3A7, Performance Test (cont)

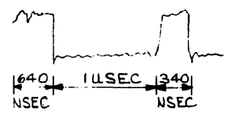
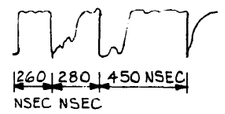
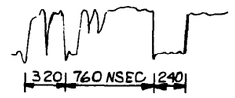
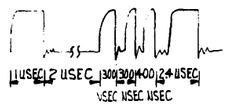
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U1-13		
		U21-13		
		U1-11		
		U21-11		

Table 6-22. CPA PC Card A1A3A7, Performance Test (cont)

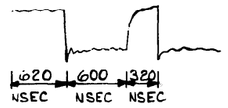
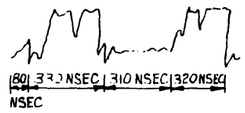
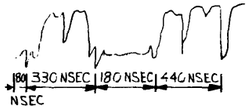
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U1-10		
		U21-10		
		U1-9		Same as U1-10
		U21-9		

Table 6-22. CPA PC Card A13A7, Performance Test (cont)

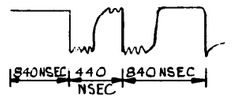
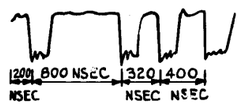
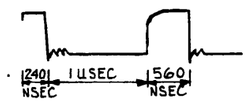
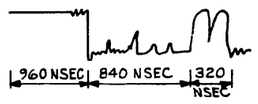
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U11-13		
		U31-13		
		U11-11		
		U31-11		

Table 6-22. CPA PC Card A1A3A7, Performance Test (cont)

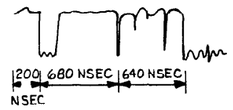
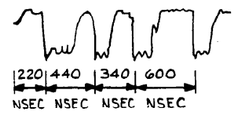
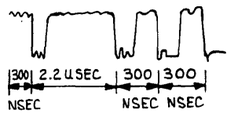
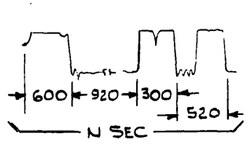
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U11-10		
		U31-10		
		U11-9		
		U31-9		

Table 6-22. CPA PC Card A1A3A7, Performance Test (cont)

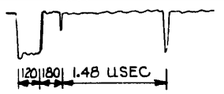
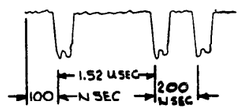
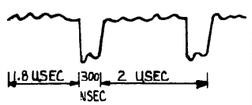
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U76-3		
		U75-8		
		U71-9		
		U71-5		0 VDC

Table 6-22. CPA PC Card A1A3A7, Performance Test (cont)

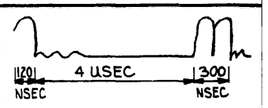
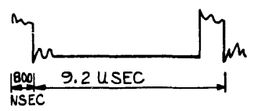
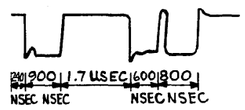
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U73-6		
		U60-15		
		U58-6		
		U58-4		

Table 6-22. CPA PC Card A1A3A7, Performance Test (cont)

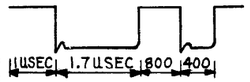
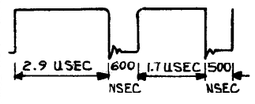
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U68-10		Same as U58-4
		U68-9		
		U58-10		
		U62-10		

Table 6-22. CPA PC Card A1A3A7, Performance Test (cont)

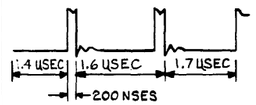
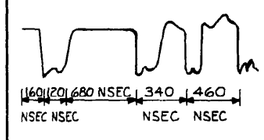
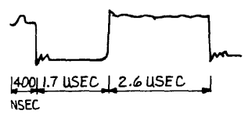
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U58-12		1.6 VDC (no signal)
		U58-2		
		U62-15		
		U58-8		

Table 6-22. CPA PC Card AlA3A7. Performance Test (cont)

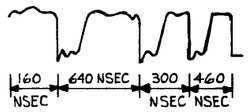
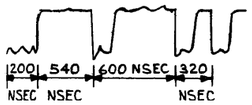
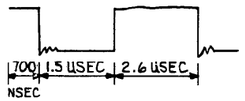
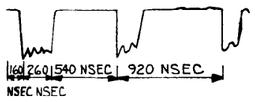
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U62-14		
		U62-13		
		U78-8		
		U62-11		

Table 6-22. CPA PC Card AlAW7, Performance Test (cont)

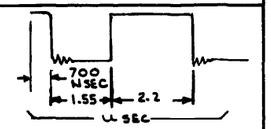
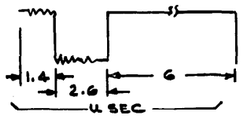
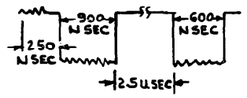
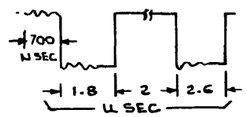
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U78-4		
		U78-2		
		U78-6		
		U68-8		

Table 6-22. CPA PC Card A1A3A7, Performance Test (cont)

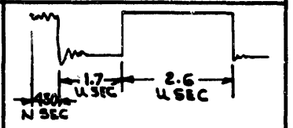
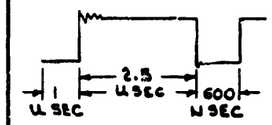
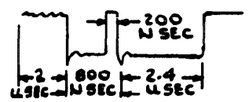
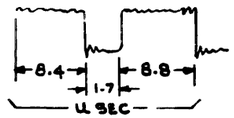
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U68-6		
		U68-2		
		U68-4		
		U36-10		

Table **6-22, CPA** PC **Card A1A3A7, Performance Test (cont)**

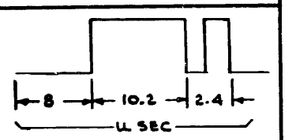
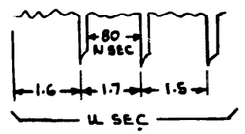
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U36-15		
		U36-9		
10			Rewind and remove ATP tape.	
11			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
12			Disconnect Interconnect Module Adapter from PC cards A1A3A5, A1A3A6, and A1A3A7.	
13			Remove CPA PC card A1A3A7 and CPB PC card A1A3A6 from card extenders.	
14			Reinstall CPA and CPB PC cards in Processor.	

Table 6-22. CPA PC Card A1A3A7, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
15			Connect Interconnect Module to PC cards A1A3A5, A1A3A6, and A1A3A7.	
16			Close Program Maintenance Panel.	
17			Secure bezel to Processor with four screws.	

a. Open Program Maintenance Panel.

b. On Processor Auto-Load PC card A1A3A9, set the four red toggle switches, designated from top to bottom as S1 through S4, as follows: Sl and S2 to up position, S3 and S4 to down position.

c. Mount and thread ATP tape on Mag Tape Unit 1 (A1A1).

d. On Mag Tape Unit, perform the following:

1. Press LOAD switch.

2. When tape movement stops press LOAD switch again.

3. When LOAD Lamp is lighted, press ON LINE switch.

4. If LOAD lamp is not lighted after the tape reel has made five or more revolutions, press REWIND switch; then, when LOAD lamp lights, press ON LINE switch.

e. Press reset and load switches.

f. When tape motion stops, repeat step e four more times to reach the fifth program (GIN 4). Tape motion must stop after each load.

g. Press run, after the fifth load.

NOTE

A loop count will appear in bits 4 to 14 and bit 2 will light to indicate GIN 4 is operating.

h. Go to step 9 of table 6-22.

6-44. CPB PC CARD COMPONENT PERFORMANCE TEST. The component performance test for the CPB PC card is used to isolate malfunctions to an IC or group of IC'S. To accomplish the CPB PC card component performance test perform the procedure in table 6-23.

6-45. After step 7 of table 6-23, load the ATP tape as follows:

a. Open Program Maintenance Panel.

b. On Processor Auto-Load PC card A1A3A9, set the four red toggle switches, designated from top to bottom as Sl through S4, as follows: Sl and S2 to up position, S3 and S4 to down position.

Mount and thread ATP tape on Mag Tape Unit 1 (A1A1).

d. On Mag Tape Unit, perform the following:

1. Press LOAD switch.

2. When tape movement stops press LOAD switch again.

3. When LOAD lamp is lighted, press ON LINE switch.

4. If LOAD lamp is not lighted after the tape reel has made five or more revolutions, press REWIND switch; then, when LOAD lamp lights, press ON LINE switch.

e. Press reset and load switches.

f. When tape motion stops, repeat step e four more times to reach the fifth program (GIN 4). Tape motion must stop after each load.

g. Press run switch after the fifth load.

NOTE

A loop count will appear in bits 4 to 14 and bit 2 will light to indicate GIN 4 is operating.

h. Go to step 9 of table 6-23.

6-46. CORE MEMORY CONTROLLER PC CARD COMPONENT PERFORMANCE TEST. The component performance test for the Core Memory Controller PC card is used to isolate malfunctions to an IC or group of IC's. To accomplish the Core Memory Controller PC card component performance test perform the procedure in table 6-24.

6-47. After step 5 of table 6-24, load the ATP tape as follows:

Table 6-23. CPB PC Card A1A3A6, Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
2			Remove four screws that secure bezel to Processor.	
3			Open Program Maintenance Panel.	
4			Remove Interconnect Module from PC cards A1A3A5, A1A3A6, and A1A3A7.	
5			Place CPB PC card A1A3A6 and CPA PC card A1A3A7 on card extenders.	
6			Connect Interconnect Module Adapter to CPB PC card A1A3A6, CPA PC card A1A3A7, and Bus Controller PC card A1A3A5.	
7			Set AC POWER 120V switch on Multiple Power Supply 1 to ON. Press POWER ALARM RESET switch on Alarm and Control Panel.	
8			Load the ATP tape as described in paragraph 6-45.	
9	Sequentially connect oscilloscope to test points and adjust to observe indicated waveform.	U71-9		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

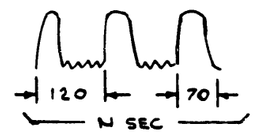
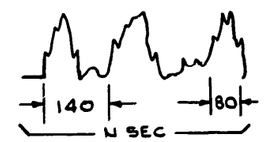
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
	NOTE Before attaching chip clip or probe to test point, press halt switch. After chip clip and/or probe is attached, press run switch. Before removing chip clip also halt program temporarily by pressing halt switch restart by pressing run switch after re-attaching chip clip and/or probe.	U72-2 U65-12 U50-12		  
		U50-10		Same as above

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

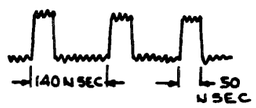
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U50-8		0 volts
		U50-2		2.4 to 5.2 VDC level
		U61-9		
		U50-4		Same as U61-9

Table 6-23. CPB PC Card A1A3A6, Performace Test (cont)

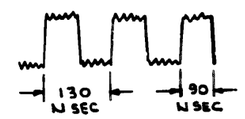
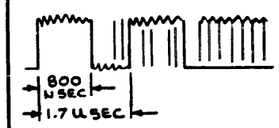
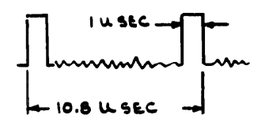
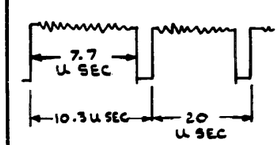
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U51-3		
		U53-2		
		U53-7		
		U53-6		

Table 6-23. CPR PC Card A1A3A6, Performance Test (cont)

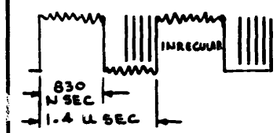
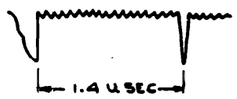
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U53-11		2.4 to 5.2 VDC level
		U53-15		
		U53-14		
		U53-1		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

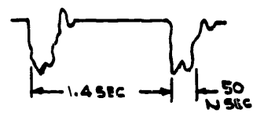
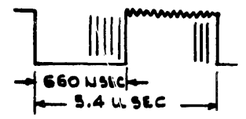
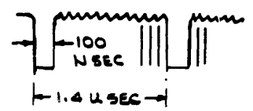
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U74-8		
		U79-8		
		U20-8		0 volts
		U74-6		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U67-8		Same as U74-6
		U79-3		0 volts
		U63-6		Same as U74-6
		U71-5		0 volts

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

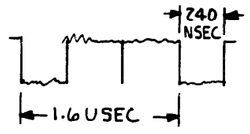
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U73-6		2.4 to 5.2 VDC level
		U62-3		0 volts
		U78-8		0 volts
		U59-6		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

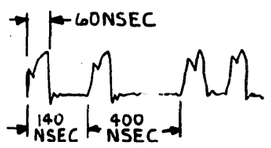
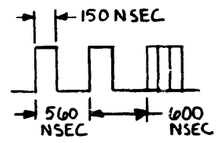
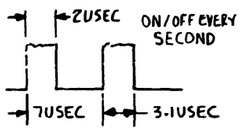
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U76-9		0 volts
		U7-12		
		U47-6		
		U1-2		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

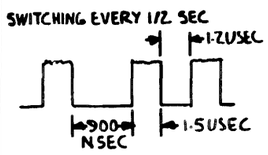
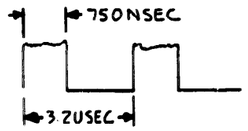
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U1-5		
		U1-7		
		U1-10		Same as U1-7
		U1-12		Same as U1-7

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

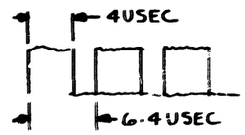
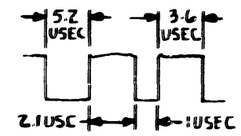
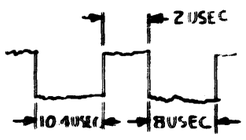
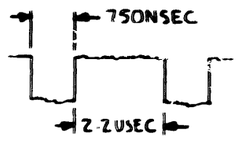
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U1-15		
		U5-2		
		U5-5		
		U5-7		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

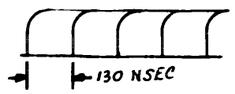
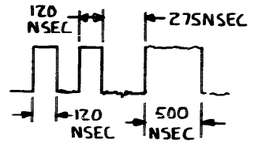
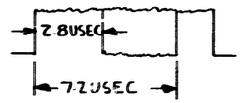
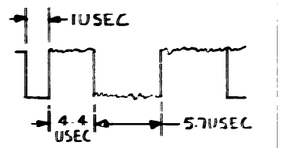
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U5-10		
		U5-12		
		U5-15		
		U3-11		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

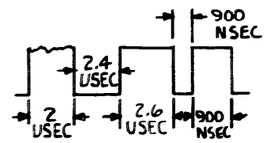
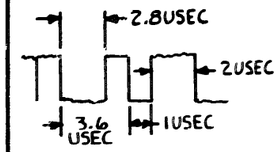
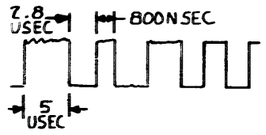
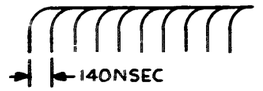
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS *
12		U3-12		
		U3-13		
		U3-14		
		U15-14		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

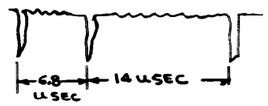
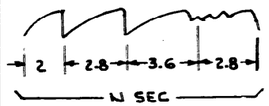
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U15-13		Same as U15-14
		U17-12		
		U16-8		
		U16-12		2.4 to 5.2 VDC level

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

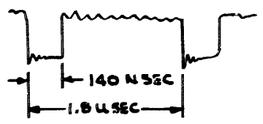
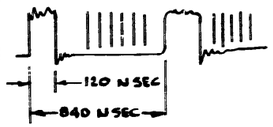
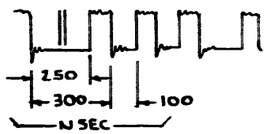
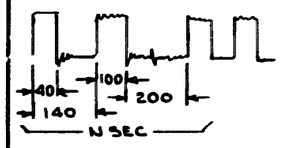
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U16-6		
		U2-7		
		U2-9		
		U4-7		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

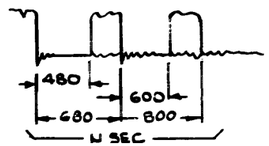
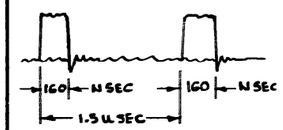
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U52-5		2.4 to 5.2 VDC level
		U37-2		
		U37-5		
		U37-7		2.4 to 5.2 VDC level

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

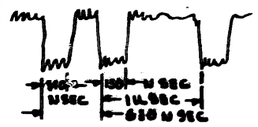
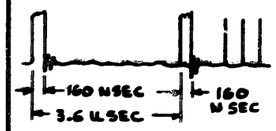
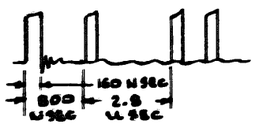
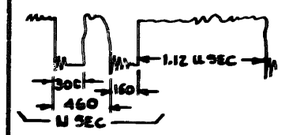
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U37-10		
		U37-12		
		U37-15		
		U38-2		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

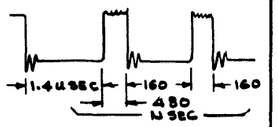
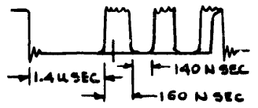
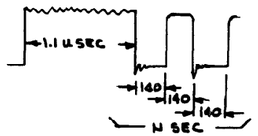
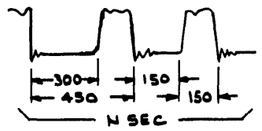
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U38-3		
		U38-7		
		U38-6		
		U38-10		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

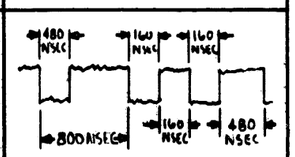
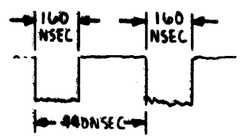
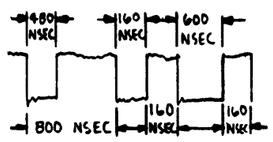
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U38-11		
		U38-15		
		U38-14		
		U40-2		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

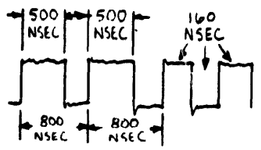
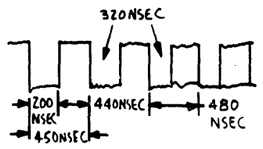
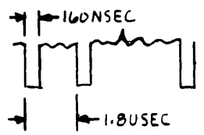
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U40-5		
		U40-7		2.4 to 5.2 VDC level
		U40-10		
		U40-12		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

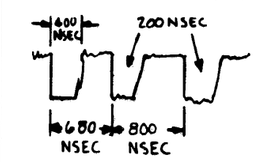
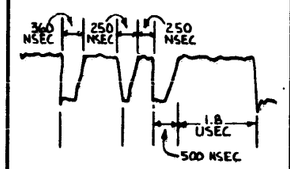
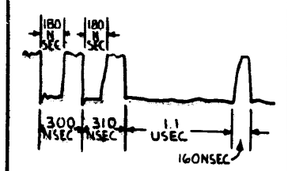
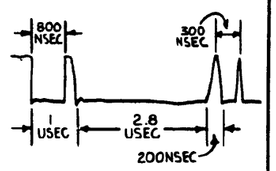
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U36-2		
		U36-5		
		U36-7		
		U36-10		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

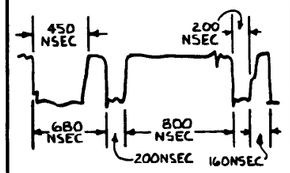
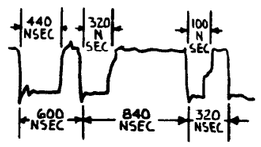
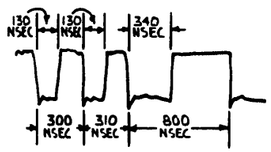
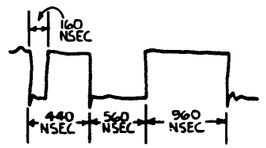
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U36-12		
		U36-15		
		U35-2		
		U35-3		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

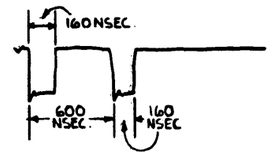
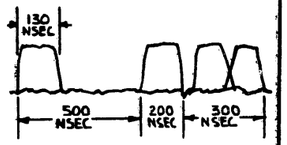
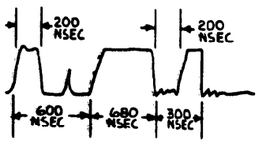
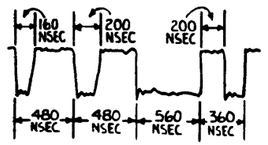
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U35-7		
		U35-6		
		U35-10		
		U35-11		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

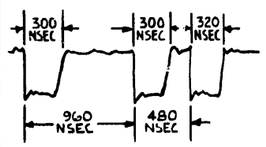
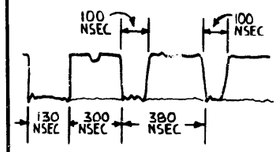
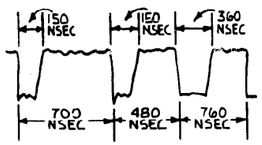
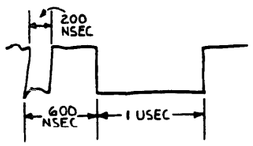
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U35-15		
		U35-14		
		U34-2		
		U34-5		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

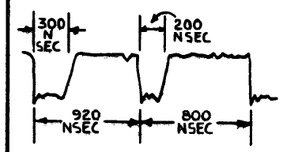
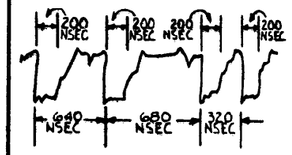
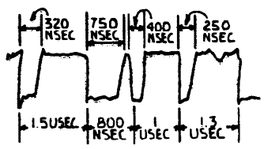
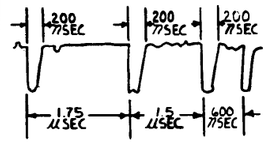
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U34-7		
		U34-10		
		U34-12		
		U34-15		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

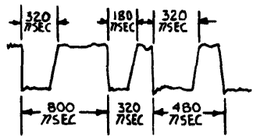
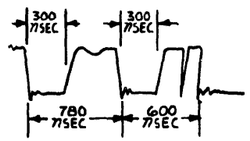
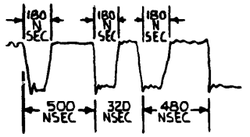
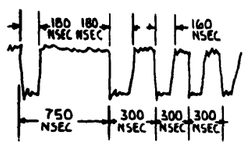
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U33-2		
		U33-3		
		U33-7		
		U33-6		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

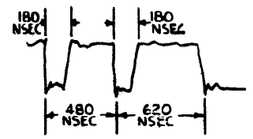
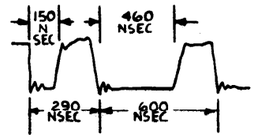
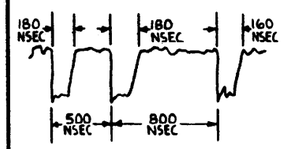
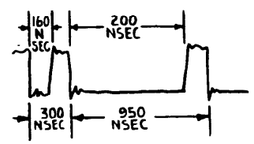
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U33-10		
		U33-11		
		U33-15		
		U33-14		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

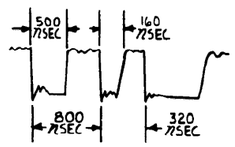
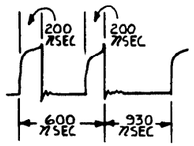
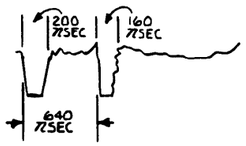
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U39-2		
		U39-3		
		U39-7		
		U39-6		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

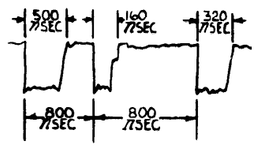
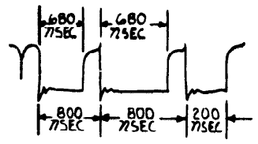
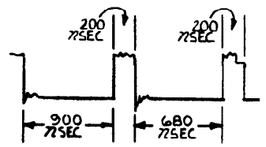
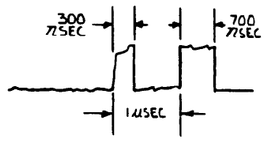
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U39-10		
		U39-11		
		U39-15		
		U43-11		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

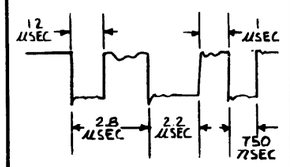
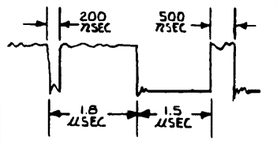
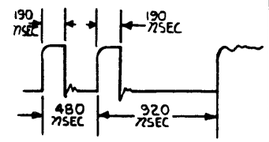
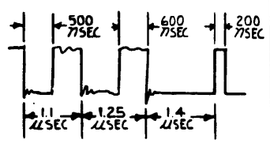
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U43-12		
		U43-13		
		U43-14		
		U44-11		

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

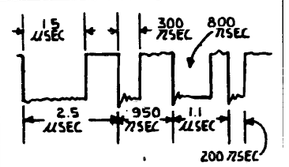
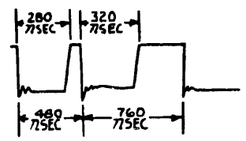
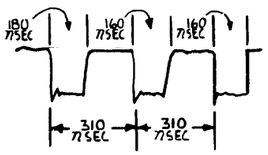
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U44-12		
		U44-13		
		U44-14		
10			Rewind and ATP tape.	
11			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
12			Disconnect Interconnect Module from PC cards A1A3A5, A1A3A6, and A1A3A7.	

Table 6-23. CPB PC Card A1A3A6, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
13			Remove PC cards A1A3A6 and A1A3A7 from card extenders.	
14			Reinstall PC cards A1A3A6 and A1A3A7 in Processor.	
15			Replace Interconnect Module ... PC cards A1A3A5, A1A3A6, and A..A3A7.	
16			Close Program Maintenance Panel.	
17			Secure bezel to Processor with four screws.	

Table 6-24. Core Memory Controller PC Card A1A3A8, Performance Test

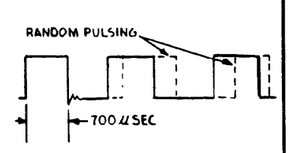
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
2			Remove four screws that secure bezel to Processor.	
3			Open Program Maintenance Panel.	
4			Place Core Memory Controller PC card A1A3A8 on card extender.	
5			Set AC POWER 120V switch on Multiple Power Supply 1 to ON. Press POWER ALARM RESET switch on Alarm and Control Panel.	
6			For instructions to load ATP tape see paragraph 6-47.	
7	Sequentially connect cscilloscope to test point and adjust to cbserve indicated waveform.	XA1-A1		

Table 6-24. Core Memory Controller PC Card A1A3A8, Performance Test (cont)

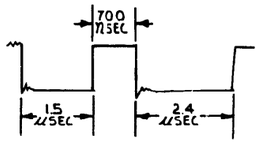
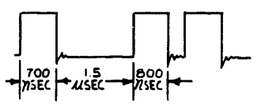
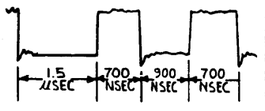
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		XA1-A2		Same as XA1-A1
		XA1-A3		
		XA1-A4		
		XA1-A5		

Table 6-24. Core Memory Controller PC Card A1A3A8, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		XA1-A6		Same as XA1-A5
		XA1-A7		Same as XA1-A5
		XA1-A8		Same as A5
		XA1-A9		Same as A5

Table 6-24. Core Memory Controller PC Card A1A3A8, Performance Test (cont)

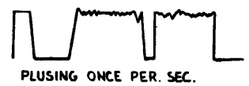
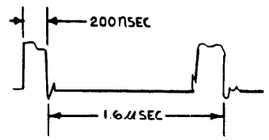
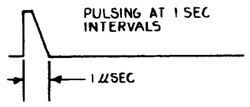
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		XA1-A10		
		XA1-A11		Same as XA1-A10
		XA1-A12		
		XA1-A13		

Table 6-24. Core Memory Controller PC Card A1A3A8, Performance Test (cont)

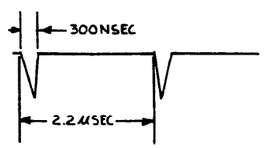
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		XA1-A14		Same as above
		XA1-A15		Same as above
		XA1-A16		0 volts
		U11-1		

Table 6-24. Core Memory Controller PC Card A1A3A8, Performance Test (cont)

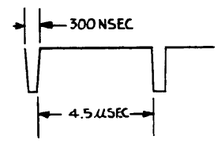
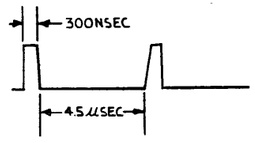
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U35-2		
		U35-7		0 volts
		U47-10		
		U47-8		

Table 6-24. Core Memory Controller PC Card A1A3A8, Performance Test (cont)

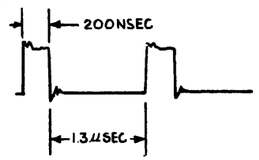
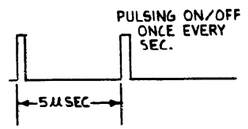
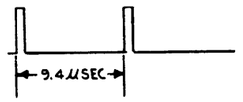
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U21-5		
		U60-12		Same as U21-5
		U46-6		
		XA1-A22		

Table 6-24. Core Memory Controller PC Card A1A3A8, Performance Test (cont)

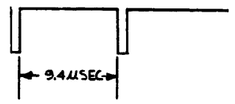
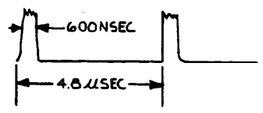
TEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		XA1-A19		Same as XA1-A22
		U62-8		
		U21-9		2.4 to 5.2 VDC level
		U47-8		

Table 6-24. Core Memory Controller PC Card A1A3A8, Performance Test (cont)

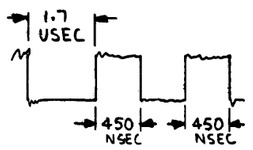
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U20-2		0 volts
		U47-2		0 volts
		XA1-A17		
		XA1-A21		Same as XA1-A22

Table 6-24. Core Memory Controller PC Card A1A3A8, Performance Test (cont)

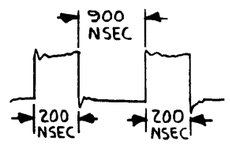
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U84-11		Same as U21-5
		U87-3		Same as U21-5
		U83-11		
		U56-6		

Table 6-24. Core Memory Controller PC Card A1A3A8, Performance Test (cont)

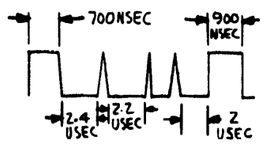
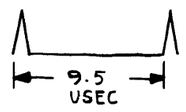
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U45-6		0 VDC
		U70-11		2.4 to 5.2 volts dc
		XA1-A25		
		XA1-A26		

Table 6-24. Core Memory Controller PC Card A1A3A8, Performance Test (cont)

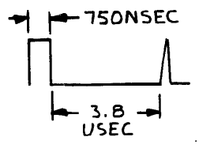
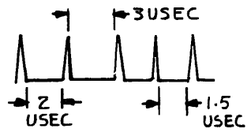
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		XA1-A28		Same as XA1-A25
		XA1-A29		
		XA1-A31		
		XA1-A32		

Table 6-24. Core Memory Controller PC Card A1A3A8, Performance Test (cont)

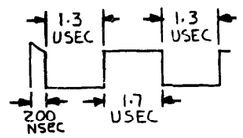
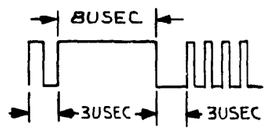
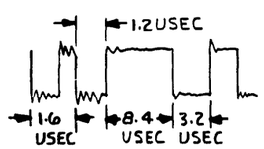
TEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U43-12		
		U43-10		
		U43-4		
		U41-11		

Table 6-24. Core Memory Controller PC Card A1A3A8, Performance Test (cont)

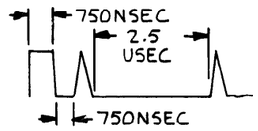
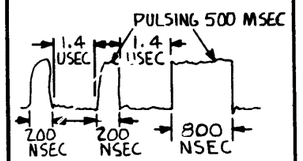
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		XA1-A40		
		XA1-A42		
		XA1-A44		Same as above
		XA1-A46		

Table 6-24. Core Memory Controller PC Card A1A3A8, Performance Test (cont)

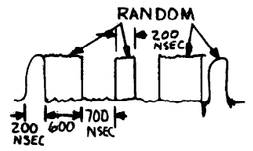
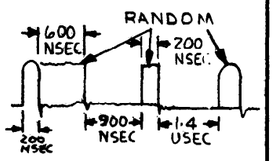
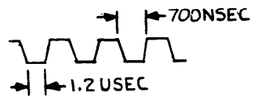
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		XA1-A48		Same as A46
		XA1-A50		
		XA1-B47		
		XA1-B49		

Table 6-24. Core Memory Controller PC Card AlA3A8, Performance Test (cont)

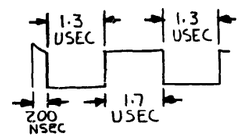
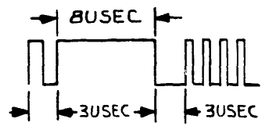
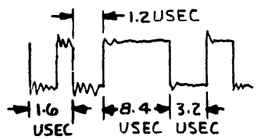
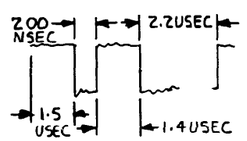
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U43-12		
		U43-10		
		U43-4		
		U41-11		

Table 6-24. Core Memory Controller PC Card A1A3A8, Performance Test (cont)

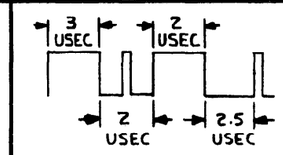
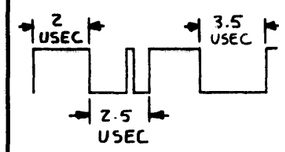
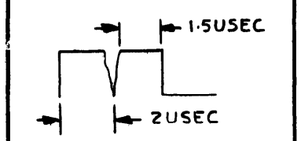
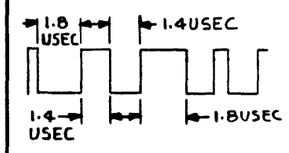
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U43-6		
		U41-12		
		U55-12		
		U55-10		

Table 6-24. Core Memory Controller PC Card A1A3A8, Performance Test (cont)

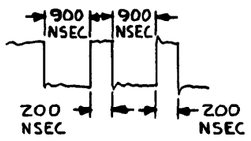
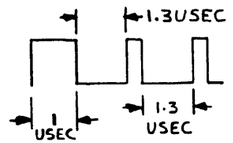
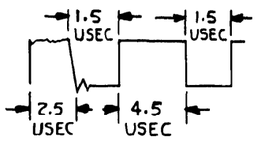
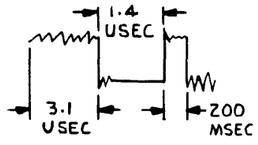
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U55-8		
		U55-2		
		U55-6		
		U55-4		

Table 6-24. Core Memory Controller PC Card A1A3A8, Performance Test (cont)

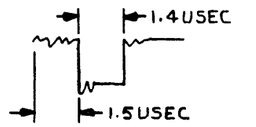
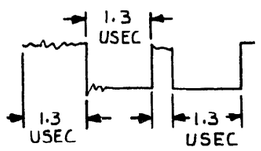
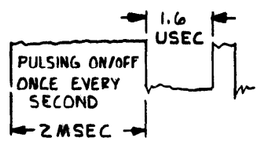
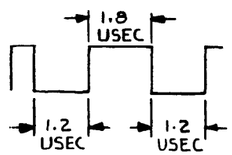
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U41-8		
		U41-2		
		U41-6		
		U41-4		

Table 6-24. Core Memory Controller PC Card A1A3A8, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
8			Rewind and remove ATP tape.	
9			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
10			Remove Core Memory Controller PC card A1A3A8 from card extender.	
11			Reinstall Core Memory Controller PC card A1A3A8 in Processor.	
12			Close Program Maintenance Panel.	

a. Open Program Maintenance Panel.

b. On Processor Auto-Load PC card A1A3A9, set the four red toggle switches, designated from top to bottom as S1 through S4, as follows: S1 and S2 to up position, S3 and S4 to down position.

Mount and thread ATP tape on Mag Tape Unit 1 (A1A1).

d. On Mag Tape Unit, perform the following:

1. Press LOAD switch.

2. When tape movement stops press LOAD **switch again.**

3. When LOAD lamp is lighted, press ON LINE switch.

4. If LOAD lamp is not lighted after the tape reel has made five or more revolutions, **press** REWIND switch; then, when LOAD **lamp** lights, press ON LINE switch.

e. Press reset and load switches.

f. When tape motion stops, repeat step e four more times to reach the fifth program (GIN 4). Tape motion must stop after each load.

g. Press run switch after the fifth load.

NOTE

A loop count will appear in bits 4 to 15 and bit 2 will light to indicate GIN 4 is operating.

h. Go to step 7 of table 6-24.

6-48. CM MIA PC CARD COMPONENT PERFORMANCE TEST. The component performance test for the CM MIA PC card is used to isolate malfunctions to an IC or group of IC'S. To accomplish the CM MIA PC card component performance test perform the procedure in table 6-25.

6-49. After step 5 of table 6-25, load the ATP tape as follows:

a. Open Program Maintenance Panel.

b. On Processor Auto-Load PC card A1A3A9, set the four red toggle switches, designated from top to bottom as S1 through **S4, as follows: S1 and S2 to up position,** S3 and S4 to down position.

c. Mount and thread ATP tape on Mag Tape Unit 1 (A1A1).

d. On Mag Tape Unit, perform the following:

1. Press LOAD switch.

2. When tape movement stops press LOAD switch again.

3. When LOAD lamp is lighted, press ON LINE switch.

4. If LOAD lamp is not lighted after the tape reel has made five or more revolutions, press REWIND switch: then, when LOAD lamp lights, press ON LINE switch.

e. **Press rest** and load switches.

f. When tape motion stops, repeat step e four more times to reach the fifth program (GIN 4). Tape motion must stop after each load.

g. Press run switch after the fifth load.

NOTE

A loop count will appear in bits 4 to 15 and bit 2 will light to indicate GIN 4 is operating.

h. Go to step 7 of table 6-25.

6-50. CM MIB PC CARD COMPONENT PERFORMANCE TEST. The component performance test for the CM MIB PC card is used to isolate malfunctions to an IC or group of IC's. To accomplish the CM MIB PC card component performance test perform the procedure in table 6-26.

6-51. After step 5 of table 6-26, load the ATP tape as follows:

Table 6-25. CM MIA PC Card A1A8A1, Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 2 to OFF.	
2			Remove four screws that secure front cover panel to Core Memory A1A8.	
3			Place CM MIA PC card A1A8A1 on card extender.	
4			Set AC POWER 120V switch on Multiple Power Supply 2 to ON.	
5			Press POWER ALARM RESET switch on Alarm and Control Panel.	
6			For instructions to mount ATP program tape see paragraph 6-49.	
7	Sequentially connect oscilloscope to test point and adjust to observe indicated waveform.	Q1-C		2.4 to 5.2 VDC level

Table **6-25. CM MIA PC Card A1ASA1, Performance Test (cont)**

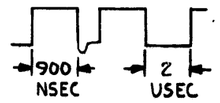
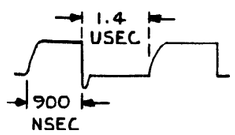
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		P1-110		
		P1-108		Same as P1-110
		P1-106		Same as P1-110
		P1-104		

Table 6-25. CM MIA PC **Card** A1ASA1, **Performance Test (cont)**

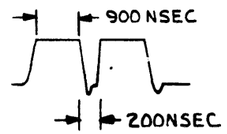
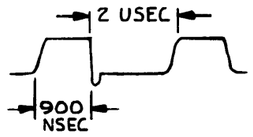
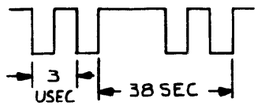
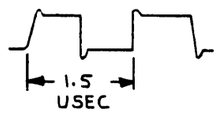
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		P1-102		
		P1-100		
		P1-52		
		P1-42		

Table 6-25. CM MIA PC Card A1A8A1, Performance Test (cont)

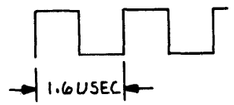
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		P1-40		Same as P1-40
		P1-38		
		P1-32		Same as P1-32
		P1-30		0 VDC

Table 6-25, CM MIA PC Card A1A8A1, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		P1-28		0 VDC
		P1-116		0 VDC
		P1-112		0 VDC
		P1-114		0 VDC

Table 6-25. CM MIA PC Card A1A8A1, Performance Test (cont)

OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
	P1-78		2.4 to 5.2 VDC level
	P1-80		0 VDC
	P1-76		0 VDC
	P1-86		0 VDC

Table 6-25. CM MIA PC Card A1A8A1, Performance Test (cont)

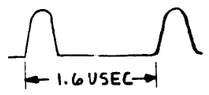
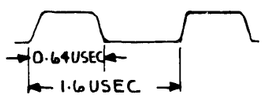
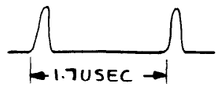
OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
	U13-6		
	U13-8		
	U18-8		
	P1-48		

Table 6-25. CM MIA PC Card A1A8A1, Performance Test (cont)

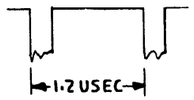
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		P1-60		Same as P1-48
		P1-54		
		P1-56		Same as P1-48
		P1-59		Same as P1-48

Table 6-25. CM MIA PC Card A1A8A1, Performance Test (cont)

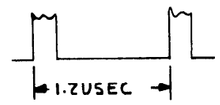
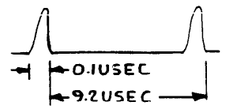
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		P1-50		
		P1-58		Same as P1-54
		P1-62		Same as P1-50
		P1-64		

Table 6-25. CM MIA PC Card A1A8A1, Performance Test (cont)

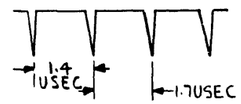
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		P1-75		
		U39-8		Same as P1-54
		U35-11		
		U26-5		2.4 to 5.2 VDC level

Table 6-25. CM MIA PC Card A1A8A1, Performance Test (cont)

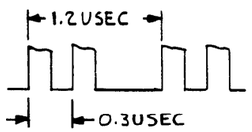
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U21-3		
		U21-11		Same as U21-3
		U16-8		
		U20-8		

Table 6-25. CM MIA PC Card A1A8A1, Performance Test (cont)

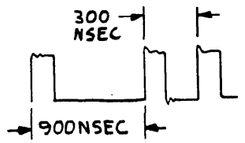
OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
	U22-6		
		Rewind and remove ATP test tape. Set AC POWER 120V switch on Multiple Power Supply 2 to OFF and reinstall CM MIA PC Card A1A8A1. Secure front cover panel to Core Memory A1A8 with four screws.	

Table 6-26. CM MIB PC Card A1A8A1, Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 2 to OFF.	
2			Remove four screws that secure front cover panel to Core Memory A1A8.	
3			Place CM MIA PC card A1A8A2 on card extender.	
4			Set AC POWER 120V switch on Multiple Power Supply 2 to ON.	
5			Press POWER ALARM RESET switch on Alarm and Control Panel.	
6			For instructions to mount ATP program tape see paragraph 6-51.	
7	Sequentially connect oscilloscope to test point and adjust to observe indicated waveform.	U29-3		

Table 6-26. CM MIB PC Card A1A8A1, Performance Test (cont)

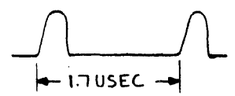
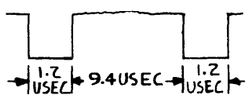
OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
	U29-11		Same as U29-3
	XA1-31		0 VDC
	XA1-109		
	U23-6		

Table 6-26. CM MIB PC Card A1A8A1, Performance Test (cont)

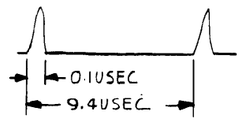
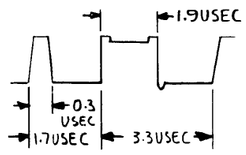
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U23-3		Same as U23-6
		U24-6		
		U24-8		Same as U24-6
		XA1-28		

Table 6-26. CM MIB PC Card A1A8A1, Performance Test (cont)

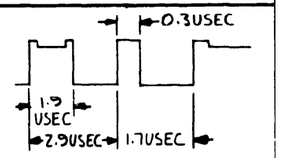
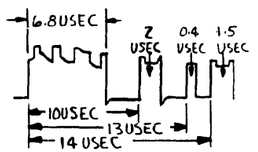
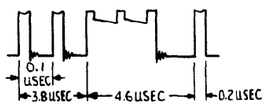
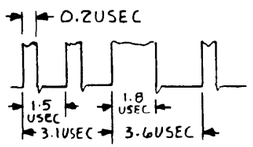
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		XA1-23		
		XA1-27		
		XA1-30		
		XA1-29		

Table 6-26. CM MIB PC Card A1A8A1, Performance Test (cont)

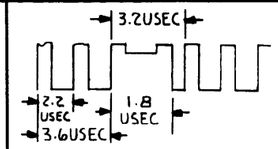
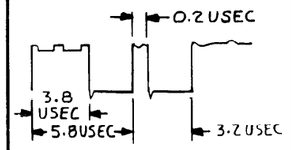
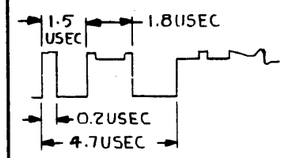
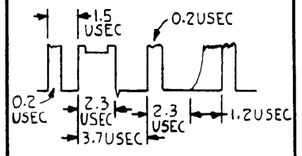
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		XA1-35		
		XA1-33		
		XA1-34		
		XA1-36		

Table 6-26. CM MIB PC Card A1A8A1, Performance Test (cont)

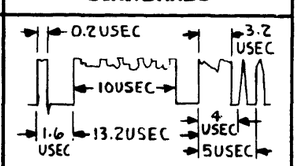
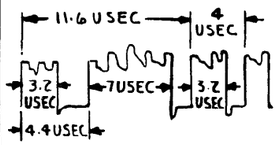
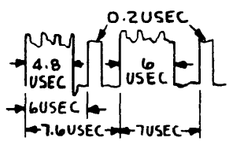
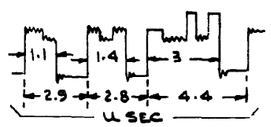
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		XA1-105		
		XA1-108		
		XA1-106		
		XA1-107		

Table 6-26. CM MIB PC Card A1A8A1, Performance Test (cont)

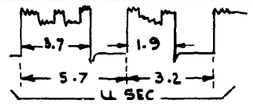
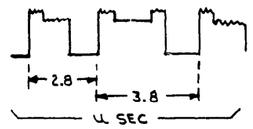
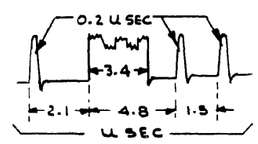
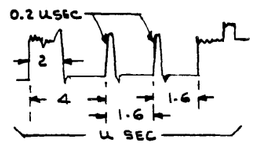
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		XA1-111		
		XA1-112		
		XA1-113		
		XA1-117		

Table 6-26. CM MIB PC Card A1A8A1, Performance Test (cont)

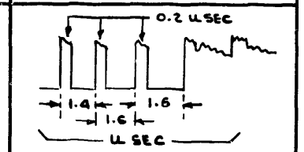
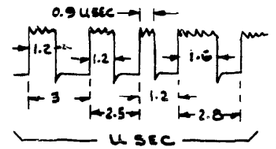
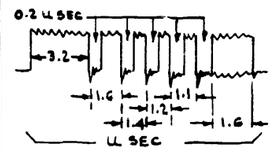
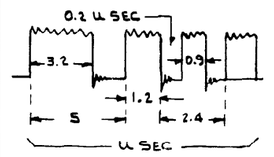
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		XA1-114		
		XA1-57		
		XA1-60		
		XA1-59		

Table 6-26. CM MIB PC Card A1F8A1, Performance Test (cont)

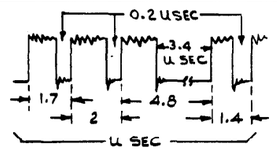
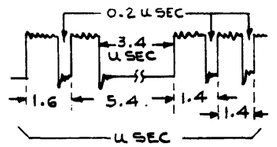
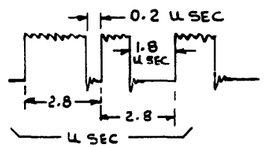
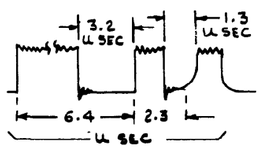
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		XA1-64		
		XA1-51		
		XA1-54		
		XA1-58		

Table 6-26. CM MIB PC Card A1A8A1, Performance Test (cont)

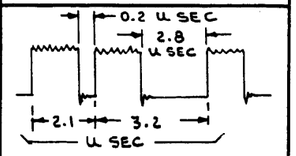
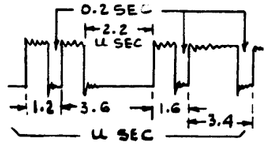
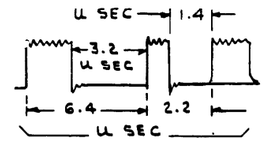
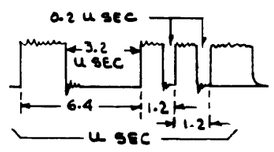
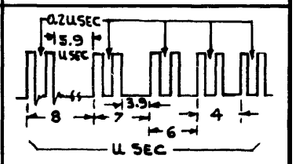
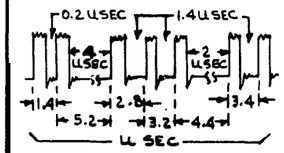
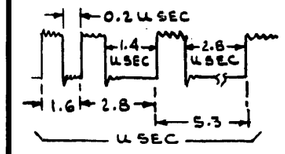
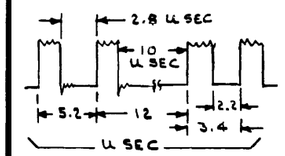
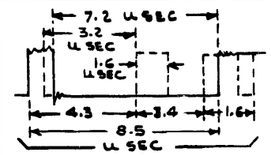
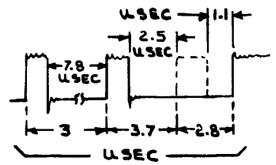
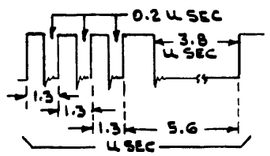
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		XA1-53		
		XA1-63		
		XA1-78		
		XA1-87		

Table 6-26. CM MIB PC Card A1A8A1, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		XA1-90		
		XA1-83		
		XA1-88		
		XA1-77		

T.O. 31S5-4-308-1
TM 11-5805-663-14-13
NAVELEX 0967-464-0010

Table 6-26. CM MIB PC Card A1A8A1, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		XA1-82		
		XA1-81		
		XA1-84		
8			Rewind and remove ATP tape.	
9			Set AC POWER 120V switch on Multiple Power Supply 2 to OFF and reinstall CM MIB PC card A1A8A2.	
10			Secure front cover panel to Core Memory A1A8 with four screws.	

a. Open Program Maintenance Panel.

b. On Processor Auto-Load **PC** card A1A3A9, set the four red toggle switches, designated from top to bottom as S1 through S4, as follows: S1 and S2 to up position, S3 and S4 to down position.

Mount and thread ATP tape on Mag Tape Unit 1 (A1A1).

d. On Mag Tape Unit, perform the following:

1. Press LOAD switch.

2. When tape movement stops press LOAD switch again.

3. When LOAD lamp is lighted, press ON LINE switch.

4. If LOAD lamp is not lighted after the tape reel has made five or more revolutions, press REWIND switch; then, when LOAD lamp lights, press ON LINE switch.

e. Press reset and load switches.

f. When tape motion stops, repeat step e four more times to reach the fifth program (GIN 4). Tape motion must stop after each load.

g. Press run switch after the fifth load.

NOTE

A loop count will appear in bits 4 to 15 and bit 2 will light to indicate GIN 4 is operating.

h. Go to step 7 of table 6-26.

6-52. CM MSA PC CARD COMPONENT PERFORMANCE TEST. The component performance test for the CM MSA PC card is used to isolate malfunctions to an IC or group of IC's. To accomplish the CM MSA PC card component performance test perform the procedure in table 6-27.

6-53. After step 6 of table 6-27, load AT? tape as follows:

a. Open Program Maintenance Panel

b. On Processor Auto-Load PC card A1A3A9, set the four red toggle switched designated from top to bottom as S1 three S4, as follows: S1 and S2 to up position S3 and S4 to down position.

Mount and thread ATP tape on Mag Tape Unit 1 (A1A1).

d. On Mag Tape Unit, perform the following:

1. Press LOAD switch.

2. When tape movement stops pre-LOAD switch again.

3. When LOAD lamp is lighted, ON LINE switch.

4. If LOAD lamp is not lighted after the tape reel has made five or more revations, press REWIND switch; then, when LOAD lamp lights, press ON LINE switch

e. Press reset and load switches.

f. When tape motion stops, repeat four more times to reach the fifth program (GIN 4). Tape motion must stop after each load.

g. Press run switch after the fifth lo

NOTE

A loop count will appear in bits 4 to 15 and bit 2 will light to indicate GIN 4 is operating.

h. Go to step 8 of table 6-27.

6-54. CM MBA PC CARD COMPONENT PERFORMANCE TEST. The component per formance test for the CM MBA PC card is used to isolate malfunctions to an IC or group of IC's. To accomplish the CM M PC card component performance test perform the procedure in table 6-28.

6-55. After step 6 of table 6-28, load the ATP tape as follows:

Table 6-27. CM MSA PC Card A1A8A3A3, A1A8A4A3, A1A8ASA3 (ACOC Group) and A1A8A3A3, A1A8A4A3, A1A8ASA3, A1A8A6A3 (Switch Group), Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 2 to OFF.	
2			Remove four screws that secure front cover panel to Core Memory A1A8.	
3			Remove CM BSM A1A8A3, A1A8A4, or A1A8A5 (ACOC Group); A1A8A3, A1A8A4, A1A8A5 or A1A8A6 (Switch Group).	
4			Place the CM BSM PC card on card extender and secure with jack screws.	
5			Set AC POWER 120V switch on Multiple Power Supply 2 to ON.	
6			Press POWER ALARM RESET switch on Alarm and Control Panel.	
7		NOTE Following test points are on CM MSA PC card.	For instructions to mount ATP program tape see paragraph 6-53.	
8	Connect multimeter to test point and adjust to observe 2.5 volt dc	Q2-C		2.5 VDC

Table 6-27. CM MSA PC Card A1A8A3A3, A1A8A4A3, A1A8ASA3 (ACOC Group) and A1A8A3A3, A1A8A4A3, A1A8ASA3, A1A8A6A3 (Switch Group), Performance Test (cont)

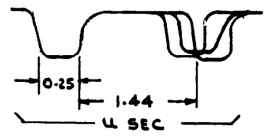
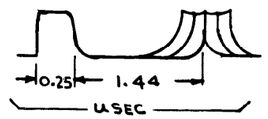
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
9	Sequentially connect oscilloscope to test point and adjust to observe indicated waveform	U49-8		
		U50-3		
		U51-3		Same as U49-8
		U50-6		Same as U50-3

Table 6-27. CM MSA PC Card A1A8A3A3, A1A8A4A3, A1A8ASA3 (ACOC Group) and A1A8A3A3, A1A8A4A3, A1A8ASA3, A1A8A6A3 (Switch Group), Performance Test (cont)

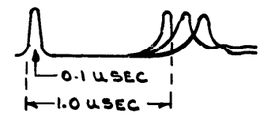
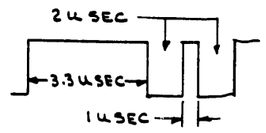
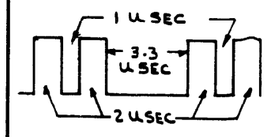
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		P1-71		
		U50-8		
		U51-8		
		J1-A17		

Table 6-27. CM MSA PC Card A1A8A3A3, A1A8A4A3, A1A8ASA3 (ACOC Group) and A1A8A3A3, A1A8A4A3, A1A8ASA3, A1A8A6A3 (Switch Group), Performance Test (cont)

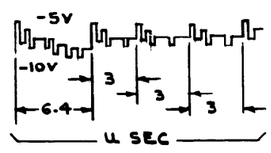
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J1-A7		Same as J1-A17
		J1-A15		Same as J1-A17
		J1-A9		Same as J1-A17
		J1-A19		

Table 6-27. CM MSA PC Card A1A8A3A3, A1A8A4A3, A1A8ASA3 (ACOC Group) and A1A8A3A3, A1A8A4A3, A1A8ASA3, A1A8A6A3 (Switch Group), Performance Test (cont)

STEP	EQUIPMENT	POINT OF TEST	OF EQUIPMENT	STANDARDS
		J1-A13		
		J1-A5		Same as J1-A17
		J1-A11		Same as J1-A17
		J1-A16		Reverse of J1-A17

Table 6-27. CM MSA PC Card A1A8A3A3, A1A8A4A3, A1A8ASA3 (ACOC Group), and A1A8A3A3, A1A8A4A3. A1A8ASA3, A1A8A6A3 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J1-A6		Reverse of J1-A17
		J1-A18		Reverse of J1-A17
		J1-A8		Reverse of J1-A17
		J1-A14		Reverse of J1-A19

Table 6-27. CM MSA PC Card A1A8A3A3, A1A8A4A3, A1A8ASA3 (ACOC Group), and A1A8A3A3, A1A8A4A3, A1A8ASA3, A1A8A6A3 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J1-A10		Reverse of J1-A13
		J1-A20		Reverse of J1-A17
		J1-A12		Reverse of J1-A17
		J1-B6		-3 VDC -6 VDC

Table 6-27. CM MSA PC Card A1A8A3A3, A1A8A4A3, A1A8ASA3 (ACOC Group), and A1A8A3A3, A1A8A4A3, A1A8ASA3, A1A8A6A3 (Switch Group), Performance Test (cont)

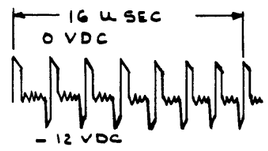
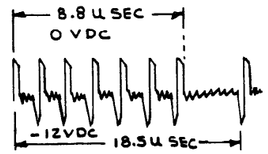
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J1-B7		Same as J1-B6
		J1-B8		
		J1-B9		
		J1-B10		-6 VDC

Table 6-27. CM MSA PC Card A1A8A3A3, A1A8A4A3, A1A8ASA3 (ACOC Group), and A1A8A3A3, A1ABA4A3. A1A8ASA3, A1A8A6A3 (Switch Group), Performance Test (cont)

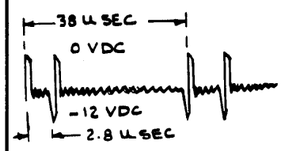
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J1-B11		
		J1-B12		-6 VDC
		J1-B13		-6 VDC
		J1-B14		-6 VDC

Table 6-27. CM MSA PC Card A1A8A3A3, A1A8A4A3, A1A8ASA3 (ACOC Group), and A1A8A3A3, A1A8A4A3, A1A8ASA3, A1A8A6A3 (Switch Group), Performance Test (cont)

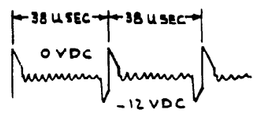
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J1-B15		-6 VDC
		J1-B16		-6 VDC
		J1-B17		-6 VDC
		J1-B18		

Table 6-27. CM MSA PC Card A1A8A3A3, A1A8A4A3, A1A8ASA3 (ACOC Group), and A1A8A3A3, A1A8A4A3. A1A8ASA3, A1A8A6A3 (Switch Group), Performance Test (cont)

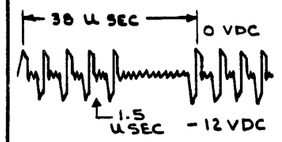
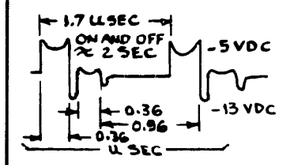
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J1-B19		
		J1-B20		-6 VDC
		J1-B21		-6 VDC
		J1-A25		

Table 6-27. CM MSA PC Card A1A8A3A3, A1A8A4A3, A1A8ASA3 (ACOC Group), and A1A8A3A3, A1A8A4A3, A1A8ASA3, A1A8A6A3 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J1-A24		Same as J1-A25
		J1-A26		Same as J1-A25
		J1-A23		Same as J1-A25
		J1-A27		Same as J1-A25

Table 6-27. CM MSA PC Card A1A8A3A3, A1A8A4A3, A1A8A5A3 (ACOC Group), and A1A8A3A3, A1A8A4A3, A1A8FSA3, A1A8A6A3 (Switch Group), Performance Test (cont)

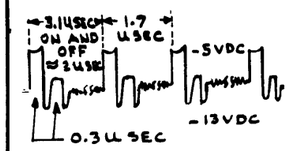
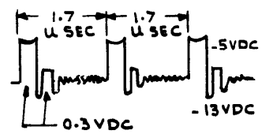
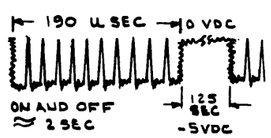
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J1-A22		
		J1-A28		
		J1-A21		Same as J1-A22
		J1-A34		

Table 6-27. CM MSA PC Card A1A8A3A3, A1A8A4A3, A1A8A5A3 (ACOC Group), and A1A8A3A3, A1A8A4A3, A1A8A5A3, A1A8A6A3 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J1-A30		Same as J1-A34
		J1-A33		Same as J1-A34
		J1-A31		Same as J1-A34
		J1-A29		Reverse of J1-A22

Table 6-27. CM MSA PC Card A1A8A3A3, A1A8A4A3, A1A8ASA3 (ACOC Group), and A1A8A.3A3, A1A8A4A3, A1A8ASA3, A1A8A6A3 (Switch Group), Performance Test (cont)

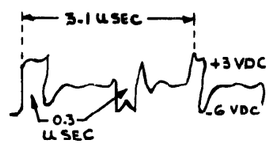
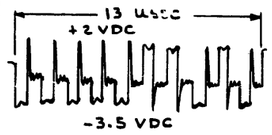
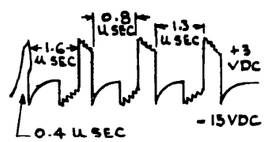
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J1-A32		
		J1-A36		
		J1-B29		-4 VDC -6 VDC
		J1-B30		

Table 6-27. CM MSA PC Card A1A8A3A3, A1A8A4A3, A1A8ASA3 (ACOC Group), and A1A8A3A3, A1A8A4A3, A1A8ASA3, A1A8A6A3 (Switch Group). Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J1-B31		Same as J1-B29
		J1-B33		Same as J1-B29
		J1-B35		Same as J1-B29
		J1-B36		Same as J1-B29

Table 6-27. CM MSA PC Card A1A8A3A3, A1A8A4A3, A1A8ASA3 (ACOC Group), and A1A8A3A3, A1A8A4A3, A1A8A5A3, A1A8A6A3 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
10			Rewind and remove ATP tape.	
11			Set AC POWER 120V switch on Muliple Power Supply 2 to OFF.	
12			Remove the CM BSM PC card from the extender and reinstall in Core Memory nest.	
13			Secure front cover panel to Core Memory A1A8 with four screws.	

Table 6-28. CM MBA PC Card A1A8A3A1, A1A8A4A1, A1A8A5Al (ACOC Group), and A1A8A3A1, A1A8A4A1, A1A8A5Al, A1A8A6Al (Switch Group) Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 2 to OFF.	
2			Remove four screws that secure front cover panel to Core Memory A1A8.	
3			Remove CM BSM A1A8A3, A1A8A4, or A1A8A5 (ACOC Group); A1A8A3, A1A8A4, A1A8A5 or A1A8A6 (Switch Group).	
4			Place the CM BSM PC card on card extender and secure with jack screws.	
5			Set AC POWER 120V switch on Multiple Power Supply 2 to ON.	
6			Press POWER ALARM RESET switch on Alarm and Control Panel.	
7			For instructions to mount ATP program tape see paragraph 6-55.	
		NOTE Following test points are on CM MBA PC card.		

Table 6-28. CM MBA PC Card A1A8A3A1, A1A8A4A1, A1A8ASAl (ACOC Group), and A1A8AW1, A1A8A4Al, A1A8ASA1, A1A8A6Al (Switch Group) Performance Test (cont)

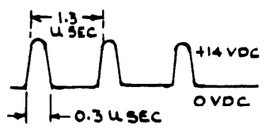
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
8	Sequentially connect oscilloscope to test point and adjust to observe indicated waveform.	Q2-C		Same as U1-6
		Q3-C		Same as U1-6
		U1-6		
		U1-3		Same as U1-6

Table 6-28. CM MBA PC Card A1A8A3A1, A1A8A4A1, A1A8A5Al (ACOC Group), and A1A8A3A1, A1A8A4A1, A1A8ASA1, A1A8A6Al (Switch Group) Performance Test (cont)

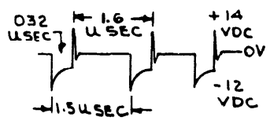
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U1-11		Same as U1-6
		J1-A20		
		J1-A19		Same as J1-A20
		J1-A18		Same as J1-A20

Table 6-28. CM MBA PC Card A1A8A3A1, A1A8A4A1, A1A8ASAl (ACOC Group), and A1A8A3A1, A1A8A4A1, A1A8ASA1, A1A8A6Al (Switch Group) Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J1-A17		Same as J1-A20
		J1-A16		Same as J1-A20
		J1-A15		Same as J1-A20
		J1-A14		Same as J1-A20

Table 6-28. CM MBA PC Card A1A8A3A1, A1A8A4A1, A1A8ASAl (ACOC Group), and A1A8A3A1, A1A8A4A1, A1A8ASA1, A1A8A6Al (Switch Group) Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J1-A13		Same as J1-A20
		A1-A12		Same as J1-A20
		J1-A11		Same as J1-A20
		J1-A28		Same as J1-A20

Table 6-28. CM MBA PC Card A1A8A3A1, A1A8A4AJ., A1A8ASAl (ACOC Group), and A1A8A3A1, A1A8A4A1, A1A8ASAl, A1A8A6A1 (Switch Group) Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J1-A27		Same as J1-A20
		J1-A26		Same as J1-A20
		J1-A25		Same as J1-A20
		J1-A24		Same as J1-A20

Table 6-28 CM MBA PC CARD A1A8A3A1, A1A8A4A1, A1A8A5A1 (ACOC Group), and A1A8AZA1, A1A8A4A1, A1A8ASA1, A1A8A6Al (Switch Group) Performance **Test (cont)**

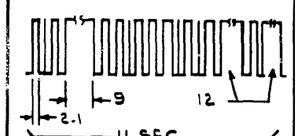
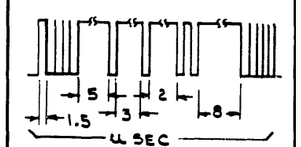
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J1-A23		Same as J1-A20
		J1-A22		Same as J1-A20
		J1-A21		Same as J1-A20
		P1-11		
		P1-15		

Table 6-28. CM MBA PC Card A1A8A3A1, A1A8A4A1, A1A8ASAl (ACOC Group), and A1A8A3A1, A1A8A4A1, A1A8A5Al, A1A8A6Al (Switch Group) Performance Test (cont)

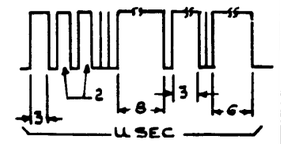
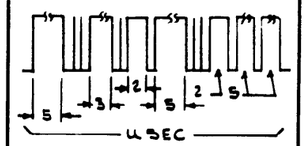
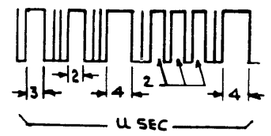
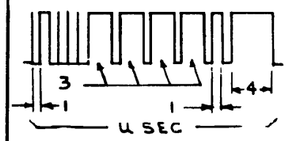
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U36-3		
		U36-6		
		U37-11		
		U37-8		

Table 6-28. CM MBA PC Card A1A8A3A1, A1A8A4A1, A1A8ASAl (ACOC Group), and A1A8A3A1, A1A8A4A1, A1A8ASA1, A1A8A6Al (Switch Group) Performance Test (cont)

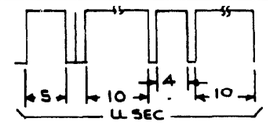
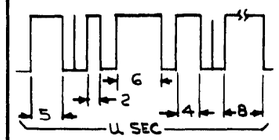
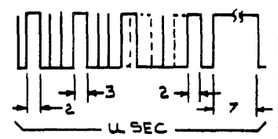
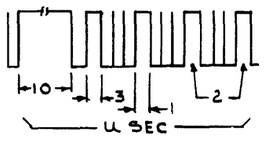
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		P1-21		
		P1-17		
		P1-93		
		U48-3		

Table 6-28. CM MBA PC Card A1A8A3A1, A1A8A4A1, A1A8ASAl (ACOC Group), and A1A8A3A1, A1A8A4A1, A1A8ASA1, A1A8A6Al (Switch Group) Performance Test (cont)

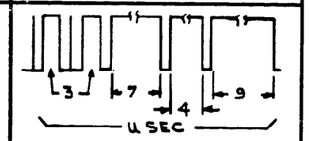
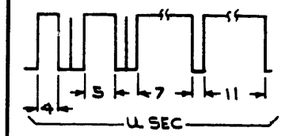
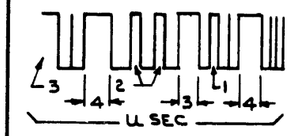
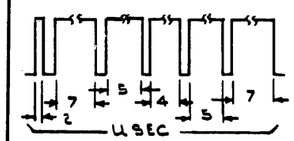
STEP	OPERATION OF TEST EQUIPMENT	FOINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		P1-119		
		U38-8		
		U38-6		
		P1-123		

Table 6-28. CM MBA PC Card A1A8A3A1, A!A8A4A1, A1A8A5A1 (ACOC Group), and A1A8A3A1, A1A8A4A1, A1A8A5A1, A1A8A6A1 (Switch Group) Performance Test (cont)

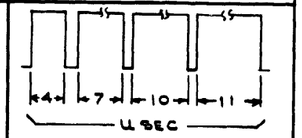
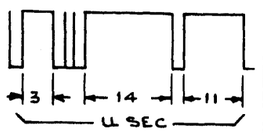
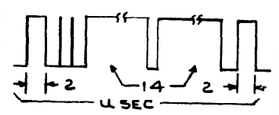
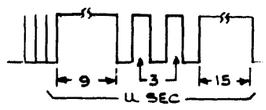
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U39-8		
		U39-11		
		P1-129		
		P1-125		

Table 6-28. CM MBA PC Card A1A8A3A1, A1A8A4A1, A1A8ASAl (ACOC Group), and A1A8A3A1, A1A8A4A1, A1A8ASA1, A1A8A6Al (Switch Group) Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
9			Rewind and remove ATP tape.	
10			Set AC POWER 120V switch on Multiple Power Supply 2 to OFF.	
11			Remove CM BSM PC card from extender card and reinstall in Core Memory nest.	
12			Secure front cover panel to Core Memory A1A8 with four screws.	

a. Open front panel (Program Maintenance Panel).

b. On Processor Auto-Load PC card A1A3A9, set the four red toggle switches, designated from top to bottom as S1 through S4, as follows: S1 and S2 to up position, S3 and S4 to down position.

Mount and thread ATP tape on Mag Tape Unit 1 (A1A1).

d. On Mag Tape Unit, perform the following:

1. Press LOAD switch.

2. When tape movement stops press LOAD switch again.

3. When LOAD lamp is lighted, press ON LINE switch.

4. If LOAD lamp is not lighted after the tape reel has made five or more revolutions, press REWIND switch; then, when LOAD lamp lights, press ON LINE switch.

e. Press reset and load switches.

f. When tape motion stops, repeat step e four more times to reach the fifth program (GIN 4). Tape motion must stop after each load.

g. Press run switch after the fifth load.

NOTE

A loop count will appear in bits 4 to 15 and bit 2 will light to indicate GIN 4 is operating.

h. Go to step 8 of table 6-28.

6-56. CM MMA PC CARD COMPONENT PERFORMANCE TEST. The component performance test for the CM MMA PC card is used to isolate malfunctions to an IC or group of IC‘s. To accomplish the CM MMA PC card component performance test perform the procedure in table 6-29. If during this performance test the malfunction is isolated to the core memory stack, the entire CM MSA PC card shall be replaced.

6-57. After step 6 of table 6-29, load ATP tape as follows:

a. Open Program Maintenance Panel.

b. On Processor Auto-Load PC card A1A3A9, set the four red toggle switches, designated from top to bottom as S1 through S4, as follows: S1 and S2 to up position, S3 and S4 to down position.

Mount and thread ATP tape on Mag Tape Unit 1 (A1A1).

d. On Mag Tape Unit, perform the following:

1. Press LOAD switch.

2. When tape movement stops press LOAD switch again.

3. When LOAD lamp is lighted, press ON LINE switch.

4. If LOAD lamp is not lighted after the tape reel has made five or more revolutions, press REWIND switch; then, when LOAD lamp lights, press ON LINE switch.

e. Press reset and load switches.

f. When tape motion stops, repeat step e four more times to reach the fifth program (GIN 4). Tape motion must stop after each load.

g. Press run switch after the fifth load.

-NOTE

A loop count will appear in bits 4 to 15 and bit 2 will light to indicate GIN 4 is operating.

h. Go to step 8 of table 6-29.

6-58. PCB PC CARD COMPONENT PERFORMANCE TEST. The component performance test for the PCB PC card is employed to isolate malfunctions to an IC or group of IC’S. To accomplish the PCB PC card component performance test perform the procedure in table 6-30.

6-59. After step 7 of table 6-30, load ATP tape as follows:

Table 6-29. CM MMA PC Card A1A8A3A2, A1A8A4A2, A1A8ASA2 (ACOC Group), and A1A8A3A2, A1A8A442, A1A8ASA2, A1A8A6A2 (Switch Group), Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 2 to OFF.	
2			Remove four screws that secure front cover panel to Core Memory A1A8.	
3			Remove CM BSM A1A8A3, A1A8A4, or A1A8A5 (ACOC Group); A1A8A3, A1A8A4, A1A8A5 or A1A8A6 (Switch Group).	
4			Place CM BSM PC card on card extender and secure with jack screws.	
5			Set AC POWER 120V switch on Multiple Power Supply 2 to ON.	
6			Press POWER ALARM RESET switch on Alarm and Control Panel.	
7			For instructions to mount test program tape see paragraph 6-57.	
		NOTE Following test points are on CM MMA PC card.		

Table 6-29. CM MMA PC Card A1A8A3A2, A1A8A4A2, A1A8ASA2 (ACOC Group), and A1A8A3A2, A1A8A4A2, A1A8ASA2. A1A8A6A2 (Switch Group). Performance Test (cont)

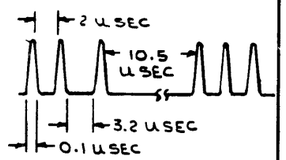
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
8	Sequentially connect multimeter to test point and adjust to observe indicated voltages.	CR5-A		-5 VDC
		CR6-A		-5 VDC
9	Sequentially connect oscilloscope to test point and observe indicated waveforms.	U4-8		
		P1-A3		

Table 6-29. CM MMA PC Card A1A8A3A2, A1A8A4A2, A1A8ASA2 (ACOC Group), and A1A8A3A2, A1A8A4A2, A1A8ASA2, A1A8A6A2 (Switch Group), Performance Test (cont)

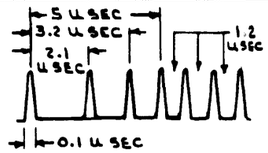
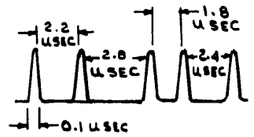
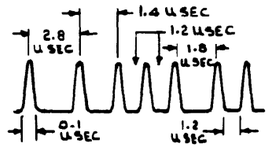
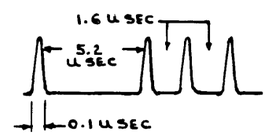
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		P1-B3		
		P1-A4		
		P1-B4		
		P1-A5		

Table 6-29. CM MMA PC Card A1A8A3A2, A1A8A4A2, A1A8ASA2 (ACOC Group), and A1A8A3A2, A1A8A4A2, A1A8ASA2, A1A8A6A2 (Switch Group). Performance Test **(cont)**

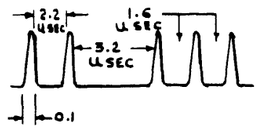
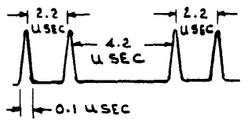
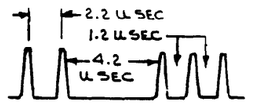
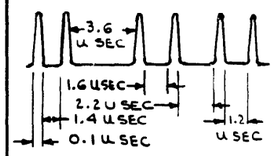
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		P1-A6		
		P1-A7		
		P1-A8		
		P1-B10		

Table 6-29. CM MMA PC Card A1A8A3A2, A1A8A4A2, A1A8ASA2 (ACOC Group), and A1A8A3A2, A1A8A4A2, A1A8ASA2, A1ASAGA (Switch Group), Performance Test (cont)

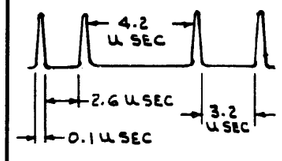
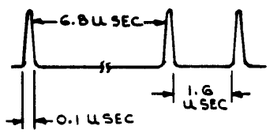
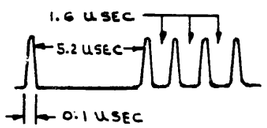
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		P1-A10		Same as P1-A8
		P1-B29		
		P1-A29		
		P1-A30		

Table 6-29. CM MMA PC Card A1A8A3A2, A1A8A4A2, A1A8ASA2 (ACOC Group), and A1A8A3A2, A1A8A4A2, A1A8A5A2, A1A8A6A2 (Switch Group). Performance Test (cont)

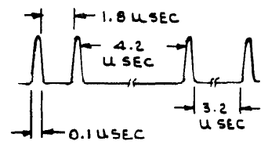
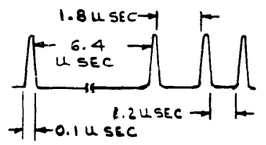
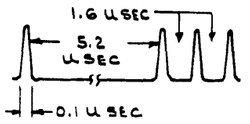
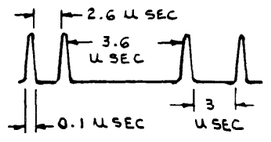
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		P1-B30		
		P1-B31		
		P1-A31		
		P1-B32		

Table 6-29. CM MMA PC Card A1A8A3A2, A1A8A4A2, A1A8A5A2 (ACOC Group), and A1A8A3A2, A1A8A4A2, A1A8ASA2, A1A8A6A2 (Switch Group), Performance Test (cont)

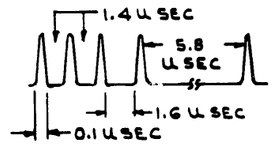
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		P1-A32		
9			Rewind and remove ATP tape.	
10			Set AC POWER 120V switch on Multiple Power Supply 2 to OFF.	
11			Remove the CM BSM PC card from the extender and reinstall in Core Memory nest.	
12			Secure front cover panel to Core Memory A1A8 with four screws.	

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
2			Remove four screws that secure bezel to front of Processor.	
3			Open Program Maintenance Panel.	
4			Remove connector P3 from PBI PC card and connectors P1 and P2 from PCB PC card.	
5			Place PBI PC card and PCB PC card on extenders. Check that interconnecting plug P4 is firmly seated.	
6			Reconnect connectors P1 and P2 to PCB PC card and connectors P3 to PBI PC card.	
7			Set AC POWER 120V switch on Multiple Power Supply 1 to ON. Press POWER ALARM RESET switch on Alarm and Control Panel.	
8			For instructions to load ATP tape see paragraph 6-59.	
9	Sequentially connect oscilloscope to test points and adjust to obtain indicated waveform.	U3-13		0 VDC

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U3-5		0 VDC
		U9-9		2.4 to 5.2 VDC level
		U9-13		0 VDC
		J4-9		0 VDC

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J4-10		0 VDC
		U14-6		0 VDC
		U14-8		2.4 to 5.2 VDC level
		U22-13		0 VDC

Table 6-30. PCB PC Card A1A3Al8 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U12-12		0 VDC
		U12-9		0 VDC
		U12-8		0 VDC
		U12-11		0 VDC

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

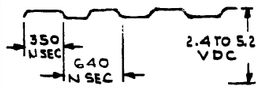
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U11-10		0 VDC
		J4-5		
		U54-8		0 VDC
		U75-12		0 VDC

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U75-4		2.4 to 5.2 VDC level
		U75-6		2.4 to 5.2 VDC level
		U75-10		2.4 to 5.2 VDC level
		U75-8		2.4 to 5.2 VDC level

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U65-6		2.4 to 5.2 VDC level
		U65-2		2.4 to 5.2 VDC level
		U65-8		2.4 to 5.2 VDC level
		U65-10		2.4 to 5.2 VDC level

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U55-4		2.4 to 5.2 VDC level
		U55-6		2.4 to 5.2 VDC level
		U55-8		2.4 to 5.2 VDC level
		U55-10		2.4 to 5.2 VDC level

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U45-4		2.4 to 5.2 VDC level
		U45-6		2.4 to 5.2 VDC level
		U45-8		2.4 to 5.2 VDC level
		U45-10		2.4 to 5.2 VDC level

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U35-6		2.4 to 5.2 VDC level
		U35-4		2.4 to 5.2 VDC level
		U35-10		2.4 to 5.2 VDC level
		U35-8		2.4 to 5.2 VDC level

Table 6-30. PCB PC Card A1A3A18, (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U25-2		2.4 to 5.2 VDC level
		U25-4		2.4 to 5.2 VDC level
		U25-10		2.4 to 5.2 VDC level
		U25-12		2.4 to 5.2 VDC level

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U15-6		2.4 to 5.2 VDC level
		U15-4		2.4 to 5.2 VDC level
		U15-8		2.4 to 5.2 VDC level
		U15-10		2.4 to 5.2 VDC level

Table 6-30. PCB PC Card A1A3F18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U5-4		2.4 to 5.2 VDC level
		U5-6		2.4 to 5.2 VDC level
		U5-10		2.4 to 5.2 VDC level
		U5-8		2.4 to 5.2 VDC level

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U72-2		2.4 to 5.2 VDC level
		U72-3		2.4 to 5.2 VDC level
		U72-4		2.4 to 5.2 VDC level
		U72-5		2.4 to 5.2 VDC level

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U72-6		2.4 to 5.2 VDC level
		U72-7		2.4 to 5.2 VDC level
		U72-8		2.4 to 5.2 VDC level
		U72-9		2.4 to 5.2 VDC level

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U72-10		2.4 to 5.2 VDC level
		U72-11		2.4 to 5.2 VDC level
		U72-13		2.4 to 5.2 VDC level
		U72-14		2.4 to 5.2 VDC level

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U72-15		2.4 to 5.2 VDC level
		U72-16		2.4 to 5.2 VDC level
		U72-17		2.4 to 5.2 VDC level
		J4-7		2.4 to 5.2 VDC level

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J4-1		0 VDC
		U76-3		2.4 to 5.2 VDC level
		U79-3		2.4 to 5.2 VDC level
		U79-6		2.4 to 5.2 VDC level

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U79-11		2.4 to 5.2 VDC level
		U79-8		2.4 to 5.2 VDC level
		U66-4		2.4 to 5.2 VDC level
		U66-12		2.4 to 5.2 VDC level

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U66-13		2.4 to 5.2 VDC level
		U56-3		0 VDC
		U56-4		0 VDC
		U56-12		0 VDC

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U56-13		0 VDC
		U46-4		0 VDC
		U46-3		0 VDC
		U46-12		0 VDC

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U46-13		0 VDC
		U29-12		2.4 to 5.2 VDC level
		U37-4		2.4 to 5.2 VDC level
		U37-1		2.4 to 5.2 VDC level

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U27-6		2.4 to 5.2 VDC level
		U27-8		2.4 to 5.2 VDC level
		U35-2		2.4 to 5.2 VDC level
		U25-6		2.4 to 5.2 VDC level

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U25-8		2.4 to 5.2 VDC level
		U37-13		2.4 to 5.2 VDC level
		U17-4		2.4 to 5.2 VDC level
		U17-1		2.4 to 5.2 VDC level

Table 6-30. PCB PC Card A1A3A18, (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U17-13		2.4 to 5.2 VDC level
		U17-10		2.4 to 5.2 VDC level
		U7-4		2.4 to 5.2 VDC level
		U7-1		2.4 to 5.2 VDC level

Table 6-30. PCB PC Card A1A3A18 (ACOC Group), A1A3A21 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U7-13		2.4 to 5.2 VDC level
		U7-10		2.4 to 5.2 VDC level
10			Rewind and remove ATP tape.	
11			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
12			Remove connector P3 from PBI PC card and P1 and P2 from PCB PC card.	
13			Reinstall PBI PC card and PCB PC card in Processor.	
14			Connect connectors P1 and P2 to PCB PC card and connector P3 to PBI PC card.	
15			Close Program Maintenance Panel.	
16			Secure bezel to Processor with four screws.	

a. Open Program Maintenance Panel.

b. On Processor Auto-Load PC card AlA3A9, set the four red toggle switches, designated from top to bottom as S1 through S4, as follows: S1 and S2 to up position, S3 and S4 to down position.

Mount and thread ATP tape on Mag Tape Unit 1 (A1A1).

d. On Mag Tape Unit, perform the following:

1. Press LOAD switch.

2. When tape movement stops press LOAD switch again.

3. When LOAD lamp is lighted, press ON LINE switch.

4. If LOAD lamp is not lighted after the tape reel has made five or more revolutions, press REWIND switch; then, when LOAD lamp lights, press ON LINE switch.

e. Press reset and then load switch.

f. When tape motion stops, repeat step e ten more times. (Tape motion must stop after each load.)

g. Press run switch.

h. The TTY shall print out:

CONTROL PANEL TP

PANEL TYPE =

i. Type in:

2220(C/R)

j. The TTY shall print out:

PANEL ADDR =

k. Type in:

FF80(C/R)

1. The TTY shall print out:

TST 1

PRESS RESET, ATTN

m. Depress reset and then attn switch.

n. The TTY shall print out:

TST 02

IF IDLE, PRESS RESET, ATTN
(ERROR **NOT** IDLE)

0. Idle lamp is lighted.

p. Go to step 9 of table 6-30.

6-60. PBI PC CARD COMPONENT PERFORMANCE TEST. The component performance test for the PBI PC card is used to isolate malfunctions to an IC or group of IC'S. To accomplish the PBI PC card component performance test perform the procedure in table 6-31.

6-61. After step 7 of table 6-31, load ATP tape as follows:

a. Open Program Maintenance Panel.

b. On Processor Auto-Load PC card A1A3A9, set the four red toggle switches, designated from top to bottom as S1 through S4, as follows: S1 and S2 to up position, S3 and S4 to down position.

Mount and thread ATP tape on Mag Tape Unit 1 (A1A1).

d. On Mag Tape Unit, perform the following:

1. Press LOAD switch.

2. When tape movement stops press LOAD switch again.

3. When LOAD lamp is lighted, press ON LINE switch.

Table 6-31. PBI PC Card A1A3A17 (ACOC Group), A1A3A20 (Switch Group), Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
2			Remove four screws that secure bezel to front of Processor.	
3			Open Program Maintenance Panel.	
4			Remove connector P3 from PBI PC card and connectors P1 and P2 from PCB PC card.	
5			Place PBI PC card and PCB PC card on card extenders. Check that interconnecting plug J4 if firmly seated.	
6			Reconnect connectors P1 and P2 to PCB PC card and connector P3 to PBI PC card.	
7			Set AC POWER 120V switch on Multiple Power Supply 1 to ON. Press POWER ALARM RESET switch on Alarm and Control Panel.	
8			For instructions to load ATP program tape see paragraph 6-61.	
9	Sequentially connect oscilloscope to test point and adjust to observe indicated waveforms.	U4-15		2.4 to 5.2 VDC level

Table 6-31. PBI PC Card A1A3A17 (ACOC Group), A1A3A20 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U4-14		0 VDC
		U4-7		0 VDC
		U4-6		2.4 to 5.2 VDC level
		U4-2		0 VDC

Table 6-31. PBI PC Card A1A3A17 (ACOC Group), A1A3A20 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U4-3		2.4 to 5.2 VDC level
		U4-10		0 VDC
		U4-11		2.4 to 5.2 VDC level
		U3-9		2.4 to 5.2 VDC level

Table 6-31. PBI PC Card A1A3A17 (ACOC Group), A1A3A20 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U3-6		2.4 to 5.2 VDC level
		J4-19		0 VDC
		J4-15		0 VDC
		U77-5		0 VDC

Table 6-31. PBI PC Card A1A3A17 (ACOC Group), A1A3A20 (Switch Group), Performance Test (cont)

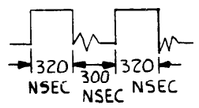
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J4-8		
		U24-6		2.4 to 5.2 VDC level
		U24-10		2.4 to 5.2 VDC level
		U24-8		0 VDC

Table 6-31. **FBI** PC Card A1A3A17 (ACOC **Group),** A1A3A20 (Switch Group), Performance Test (cont)

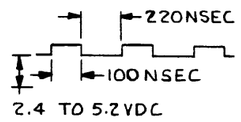
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U53-8		0 VDC
		U43-3		
		U2-8		2.4 to 5.2 VDC level
		U52-8		2.4 to 5.2 VDC level

Table 6-31. PBI PC Card A1A3A17 (ACOC Group), A1A3A20 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U43-8		2.4 to 5.2 VDC level
		U54-5		0 VDC
		U54-9		0 VDC
		U45-6		2.4 to 5.2 VDC level

Table 6-31. PBI PC Card A1A3A17 (ACOC Group), A1A3A20 (Switch Group), Performance Test (cont)

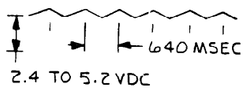
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U14-5		0 VDC
		U65-5		0 VDC
		U65-8		2.4 to 5.2 VDC level
		U63-12		

Table 6-31. PBI PC Card A1A3A17 (ACOC Group), A1A3A20 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U63-8		2.4 to 5.2 VDC level
		U63-6		Same as U43-3
		U62-6		Same as U43-3
		U42-8		2.4 to 5.2 VDC level

Table 6-31. PBI PC Card A1A3A17 (ACOC Group), A1A3A20 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U25-6		2.4 to 5.2 VDC level
		U52-12		2.4 to 5.2 VDC level
		U6-6		0 VDC
		U13-8		0 VDC

Table 6-31. PBI PC Card A1A3A17 (ACOC Group), A1A3A20 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U42-12		0 VDC
		U23-8		0 VDC
		U42-10		2.4 to 5.2 VDC level
		U25-11		2.4 to 5.2 VDC level

Table 6-31. PBI PC Card A1A3A17 (ACOC Group), A1A3A20 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U64-3		0 VDC
		U64-6		2.4 to 5.2 VDC level
		J4-18		0 VDC
		J4-17		0 VDC

Table 6-31. PBI PC Card A1A3A17 (ACOC Group), A1A3A20 (Switch Group), Performance Test (cont)

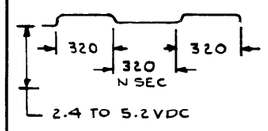
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J4-11		0 VDC
		J4-12		2.4 to 5.2 VDC level
		J4-6		0 VDC
		J4-3		

Table 6-31. PBI PC Card A1A3A17 (ACOC Group), A1A3A20 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J3-28		2.4 to 5.2 VDC level
		J3-10		2.4 to 5.2 VDC level
		J4-22		0 VDC
		U70-11		2.4 to 5.2 VDC level

Table 6-31. PBI PC Card A1A3A17 (ACOC Group), A1A3A20 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U66-6		0 VDC
		J3-4		2.4 to 5.2 VDC level
		J3-6		0 VDC
		J3-8		2.4 to 5.2 VDC level

Table 6-31. PBI PC Card A1A3A17 (ACOC Group), A1A3A20 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J4-21		0 VDC
		J4-2		0 VDC
		U58-12		2.4 to 5.2 VDC level
		U58-8		2.4 to 5.2 VDC level

Table 6-31. PBI PC Card A1A3A17 (ACOC Group), A1A3A20 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U68-8		0 VDC
		U47-8		0 VDC
		U48-8		2.4 to 5.2 VDC level
		U38-8		2.4 to 5.2 VDC level

Table 6-31. PBI PC Card A1A3A17 (ACOC Group), A1A3A20 (Switch Group), Performance Test (cont)

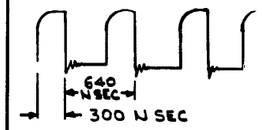
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J4-4		
		J4-23		0 VDC
		U16-3		0 VDC
		J4-24		0 VDC

Table 6-31. PBI PC Card A1A3A17 (ACOC Group), A1A3A20 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U46-9		0 VDC
		U46-5		0 VDC
		U26-11		0 VDC
		U20-8		2.4 to 5.2 VDC level

Table 6-31. PBI PC Card A1A3A17 (ACOC Group), A1A3A20 (Switch Group), Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J3-44		2.4 to 5.2 VDC level
10			Rewind and remove ATP tape.	
11			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
12			Remove connector P3 from PBI PC card and P1 and P2 from PCB PC card.	
13			Reinstall PBI PC card and PCB PC card in Processor.	
14			Connect connectors P1 and P2 to PCB PC card and connector P3 to PBI PC card.	
15			Close Program Maintenance Panel.	
16			Secure bezel to Processor with four screws.	

4. If LOAD lamp is not lighted after the **tape** reel has made five or more revolutions, press REWIND switch: then, when LOAD lamp lights, press ON LINE switch.

e. Press reset and, then load switch.

f. When tape motion stops, repeat step e ten more times. (Tape motion must stop after each load.)

g. Press run switch.

h. The TTY shall print out:

CONTROL PANEL TP

PANEL TYPE =

i. Type in:

2220(C/R)

j The TTY shall print out:

PANEL ADDR =

k. Type in:

FF80(C/R)

1. The TTY shall print out:

TST 1

PRESS RESET, ATTN

m. Depress reset and then attn switch.

n. The TTY shall print out:

TST 02

IF IDLE, PRESS RESET, ATTN
(ERROR NOT IDLE)

0. Idle lam;, is lighted.

p. **Go** to step 9 of table 6-31.

6-62. TTY CONTROLLER PC CARD COMPONENT PERFORMANCE TEST. The component Performance test for the TTY Controller PC card is used ***to*** isolate malfunctions to an IC or group of IC's. To accomplish the TTY Controller PC card component performance test perform the procedure in table 6-32.

6-63. After step 5 of table 6-32, load the ATP test tape as follows:

a. Open Program Maintenance Panel.

b. On Processor Auto-Load PC card A1A3A9, set the four red toggle switches, designated from top to bottom as S1 through S4, as follows: S1 and S2 to up position, S3 and S4 to down position.

Mount and thread ATP tape on Mag Tape Unit 1 (A1Al).

d. On Mag Tape Unit, perform the following:

1. Press LOAD switch.

2. When tape movement stops press LOAD switch again.

3. When LOAD lamp is lighted, press ON LINE switch.

4. If LOAD lamp is not lighted after the tape reel has made five or more revolutions, press REWIND switch; then, when LOAD lamp lights, press ON LINE switch.

e. Press reset and load switch.

f. When tape motion stops, repeat step e eleven more times, to reach the twelfth program. (Tape motion must come to a stop after each load.)

g. Press run switch.

h. The TTY shall print out:

TTY TEST

TTY LEV =

1. Type in:

2 (C/R)

Table 6-32. TTY Controller PC Card A1A3A11, Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
2			Remove four screws that secure bezel to Processor.	
3			Open Program Maintenance Panel.	
4			Place TTY Controller PC card A1A3A11 on card extender.	
5			Set AC POWER 120V switch on Multiple Power Supply 1 to ON. Press POWER ALARM RESET switch on Alarm and Control Panel.	
6			For instructions to load ATP tape see paragraph 6-63.	
7	Connect multimeter to test point and adjust to read -12 volts dc level.	Q1-E		Observe that voltage level is -12 ±2 volts dc.
8	Connect multimeter to test point and adjust to read 12 volts dc level.	Q2-E		Observe that voltage le level is +12 ±2 volt dc.

Table 6-32. TTY Controller PC Card A1A3A11, Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF. Remove four screws that secure bezel to Processor. Open Program Maintenance Panel. Place TTY Controller PC card A1A3A11 on card extender. Set AC POWER 120V switch on Multiple Power Supply 1 to ON. Press POWER ALARM RESET switch on Alarm and Control Panel. For instructions to load ATP tape see paragraph 6-63.	
	Connect multimeter to test point and adjust to read -12 volts dc level.	Q1-E		Observe that voltage level is -12 ±2 volts dc.
	Connect multimeter to test point and adjust to read 12 volts dc level.	Q2-E		Observe that voltage le level is +12 ±2 volt dc.

Table 6-32. TTY Controller PC Card A1A3A11, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
9	Sequentially connect multimeter to test point and adjust to read 5 volts dc level.	U38-10		Observe the voltage level is between 2.4 volts dc and 5.2 volts dc at all test points.
		U38-12		
		U38-3		
		U50-6		

Table 6-32. TTY Controller PC Card A1A3A11, Performance Test (cont)

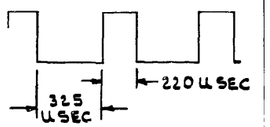
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U50-12		
		U50-10		
10	Connect multimeter to test point and adjust to read 0 volt dc level.	U50-8		Observe that voltage level is between 0.0 volt dc and 0.4 volt dc.
11	Sequentially connect oscilloscope to test point and adjust to observe indicated waveform.	U61-3		

Table 6-32. TTY Controller PC Card A1A3A11, Performance Test (cont)

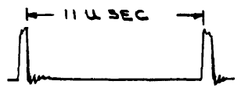
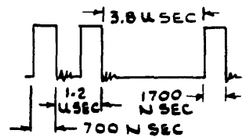
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U36-9		
		U2-8		
		U1-8		0 VDC
		U4-12		Same as U36-9

Table 6-32. TTY Controller PC Card A1A3A11, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U4-4		0 volts
		U55-6		0 volts
		U55-3		Same as U36-9
		U34-12		0 volts

Table 6-32. TTY Controller PC Card A1A3A11, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U24-8		0 volts dc
		U33-8		2.4 to 5.2 VDC level
		U61-5		2.4 to 5.2 VDC level
		U36-6		2.4 to 5.2 VDC level

Table 6-32. TTY Controller PC Card A1A3A11, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U33-11		2.4 to 5.2 VDC level
		U35-8		Same as U36-9
		U26-12		
		U48-6		2.4 to 5.2 VDC level

Table 6-32. TTY Controller PC Card A1A3A11, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U48-3		2.4 to 5.2 VDC level
		U4-2		0 volts
		U4-10		2.4 to 5.2 VDC level
		U68-6		0 volts

Table 6-32. TTY Controller PC Card A1A3A11, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U53-14		2.4 to 5.2 VDC level
		U41-11		2.4 to 5.2 VDC level
		U51-6		2.4 to 5.2 VDC level
		U32-8		2.4 to 5.2 VDC level

Table 6-32. TTY Controller PC Card A1A3A11, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U41-6		2.4 to 5.2 VDC level
		U57-8		2.4 to 5.2 VDC level
		U77-20		0 VDC
		U77-18		0 VDC

Table 6-32. TTY Controller PC Card A1A3A11, Performance Test (cont)

TEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U77-16		0 VDC
		U77-14		0 VDC
		U77-10		0 VDC
		U77-8		0 VDC

Table 6-32. TTY Controller PC Card A1A3A11, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U77-6		0 VDC
		U77-4		0 VDC
		U66-6		2.4 to 5.2 VDC level
		J1-A5		-9 VDC

Table 6-32. TTY Controller PC Card A1A3A11, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J1-B7		+13 VDC
		J1-B3		+13 VDC
		U23-3		0 volts
		U16-8		0 volts

Table 6-32. TTY Controller PC Card A1A3A11, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U16-3		2.4 to 5.2 VDC level
		U15-6		0 volts
		U25-8		2.4 to 5.2 VDC level
		U15-8		2.4 to 5.2 VDC level

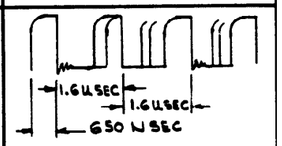
Table 6-32. TTY Controller PC Card A1A3A11, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U78-9		Same as U36-9
		U78-7		Same as U36-9
		U67-9		Same as U36-9
		U67-7		Same as U36-9

Table 6-32. TTY Controller PC Card A1A3A11, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U58-9		Same as U36-9
		U58-7		Same as U36-9
		U56-9		2.4 to 5.2 VDC level
		U56-7		0 VDC

Table 6-32. TTY Controller PC Card A1A3A11, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U29-12		
		U40-2		2.4 to 5.2 VDC level
12			Rewind and remove ATP test tape.	
13			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
14			Remove TTY Controller PC card A1A3A11 from card extender.	
15			Reinstall TTY Controller PC card A1A3A11 in Processor.	
16			Close Program Maintenance Panel.	
17			Secure bezel to Processor with four screws.	

j. The TTY shall print out:

TTY ADD =

k. Type in either:

F8OO(C/R)

1. The TTY shall print out:

BTA = (YES = l, NO = O)

m. On Program Maintenance Panel:

1. Enter hexidecimal 100 in address line.

2. Enter hexidecimal 4004 in data line.

n. Type in:

0(C/R)

o. The TTY shall print out:

TST 01

p. When TEST 01 starts, immediately press write switch in address line.

q. Turn off TTY power switch.

r. Go to step 7 of table 6-32.

6-64. MAG TAPE CONTROLLER PC CARD COMPONENT PERFORMANCE TEST. The component performance test for the Mag Tape Controller PC card is used to isolate malfunctions to an IC or group of IC's. To accomplish the Mag Tape Controller PC card component performance test perform the procedure in table 6-33.

6-65. After step 7 of table 6-33, load the ATP test tape as follows:

a. Open front panel (Program Maintenance Panel).

b. On Processor Auto-Load PC card A1A3A9, set the four red toggle switches, designated from top to bottom as S1 through S4, as follows: S1 and S2 to up position, S3 and S4 to down position.

Mount and thread ATP tape on Mag Tape Unit 1 (A1A1).

d. On Mag Tape Unit, perform the following:

1. Press LOAD switch.

2. When tape movement stops press LOAD switch again.

3. When LOAD lamp is lighted, press ON LINE switch.

4. If LOAD lamp is not lighted after the tape reel has made five or more revolutions, press REWIND switch; then, when LOAD lamp lights, press ON LINE switch.

e. Press reset and load switch.

f. When tape motion stops repeat step e twelve more times, to reach the thirteenth program (tape motion must come to a stop after each load).

g. Press run switch.

h. The TTY shall print out:

SUE MAG TAPE (BTA) TP

R/R OR C (1 or 0) =

i. Type in:

1(C/R)

j. The TTY shall print out:

ADDR =

k. Type in:

F8C0(C/R)

1. The TTY shall print out:

LVL =

Table 6-33, Mag Tape Controller PC Card A1A3A14, Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
2			Remove four screws that secure bezel to Processor.	
3			Open Program Maintenance Panel.	
4			Remove front edge connector from Mag Tape Controller PC card A1A3A14.	
5			Place Mag Tape Controller PC card A1A3A14 on card extender.	
6			Remove four screws holding the Formatter nest A1A2 and pull the nest forward about six inches; reconnect edge-connector to Mag Tape Controller PC card A1A3A14. NOTE If edge-connector does not reach PC card A1A3A14, remove two screws holding cable support bar. This will allow nest to be pulled further forward.	
7			Set AC POWER 120V switch on Multiple Power Supply 1 to ON. Press POWER ALARM RESET switch on Alarm and Control Panel.	

Table 6-33. Mag Tape Controller PC Card A1A3A14, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
8			For instructions to load ATP tape see paragraph 6-65.	
9	Sequentially connect multimeter to test points and adjust to indicate 5 volts dc.	U9-6		Observe that multimeter indicates voltage level between 2.4 volts dc and 5.2 volts dc.
		U27-10		
		U27-4		
10	Sequentially connect multimeter to test points and adjust to indicate 0 volt dc.	U9-4		Observe that multimeter indicates voltage level between 0.0 volt dc and 0.4 volt dc.

Table 6-33. Mag Tape Controller PC Card A1A3A14, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U9-2		
		U27-8		
		U27-12		
		U27-6		

Table 6-33. Mag Tape Controller PC Card A1A3A14, Performance Test (cont.)

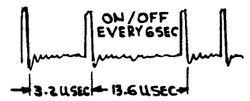
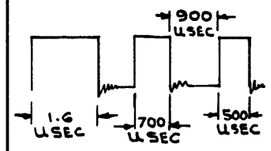
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
11	Sequentially connect oscilloscope to test point and adjust to display indicated waveform.	U18-5		
		U8-8		
		U7-8		0 VDC
		U7-6		Reverse of U18-5

Table 6-33. Mag Tape Controller PC Card A1A3A14, Performance Test (cont)

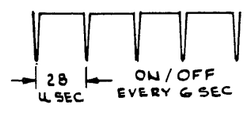
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U3-8		0 VDC
		U17-8		Same as U18-5
		U17-11		0 VDC
		U64-8		

Table 6-33. Mag Controller PC Caard A1A3A14, Performance Test (cont)

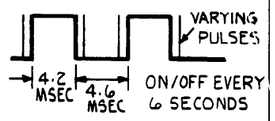
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J2-A17		2.4 to 5.2 VDC on/off every 6 sec
		J2-A16		
		J2-A15		Same as J2-A16
		J2-A13		Same as J2-A16

Table 6-33. Mag Tape Controller PC Card A1A3A14, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J2-A12		Same as J2-A16
		J2-A11		2.4 to 5.2 VDC ON/OFF every 6 sec
		J2-A10		2.4 to 5.2 VDC ON/OFF every 6 sec
		E14		0 VDC

Table 5-33. Mag Tape Controller PC Card A1A3A14, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		E15		0 VDC
		E40		2.4 to 5.2 VDC level
		E39		2.4 to 5.2 VDC level
		E41		2.4 to 5.2 VDC level

Table 6-33. Mag Tape Controller PC Card A1A3A14, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		E42		2.4 to 5.2 VDC level
		E43		2.4 to 5.2 VDC level
		E44		2.4 to 5.2 VDC level
		U65-6		0 VDC

Table 6-33. Mag Tape Controller PC Card A1A3A14, Performance Test (cont)

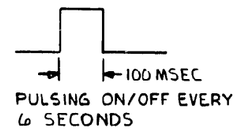
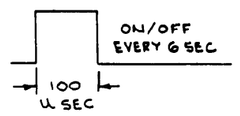
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U74-8		2.4 to 5.2 VDC level
		U65-4		
		U65-12		
		U65-10		2.4 to 5.2 VDC (ON/ OFF every 6 sec)

Table 6-33. Mag Tape Controller PC Card A1A3A14, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U65-8		2.4 to 5.2 VDC level
		U69-2		2.4 to 5.2 VDC level
		E13		0 VDC
		J2-A7		2.4 to 5.2 VDC level

Table 6-33. Mag Tape Controller PC Card A1A3A14, Performance Test (cont)

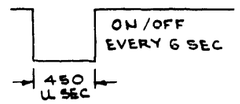
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U15-6		
		U21-6		0 VDC
		U13-8		2.4 to 5.2 VDC level
		U31-6		2.4 to 5.2 VDC level

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Table 6-33. Mag Tape Controller PC Card A1A3A14, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U27-2		2.4 to 5.2 VDC level
		J2-A5		2.4 to 5.2 VDC level
		J2-A6		2.4 to 5.2 VDC ON/OFF every 6 sec.
		U2-4		2.4 to 5.2 VDC level

Table 6-33. Mag Tape Controller PC Card A1A3A14, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J2-A8		2.4 to 5.2 VDC level
		J2-A9		2.4 to 5.2 VDC level
		U42-13		0 VDC
		U33-3		0 VDC

Table 6-33. Mag Tape Controller PC Card A1A3A14, Performance Test (cont)

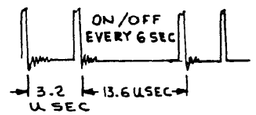
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U36-6		2.4 to 5.2 VDC level
		U49-7		2.4 to 5.2 VDC (ON/OFF every 6 sec)
		U49-9		
		U48-9		Reverse of U49-9

Table 6-33. Mag Tape Controller PC Card A1A3A14, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U48-7		2.4 to 5.2 VDC level
		U59-9		2.4 to 5.2 VDC level
		U59-7		2.4 to 5.2 VD
		U58-9		Reverse of U49-9

Table 6-33. Mag Tape Controller PC Card A1A3Al4, Performance Test (cont)

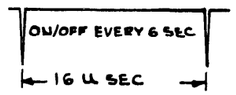
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U58-7		Same as U49-9
		U68-4		
		U68-7		Same as U68-4
		U68-12		2.4 to 5.2 VDC level

Table 6-33. Mag Tape Controller PC Card A1A3A14, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U68-9		2.4 to 5.2 VDC level
		U78-9		2.4 to 5.2 VDC level
		U78-12		2.4 to 5.2 VDC level
		U78-4		2.4 to 5.2 VDC level

Table 6-33. Mag Tape Controller PC Card A1A3A14, Performance Test (cont)

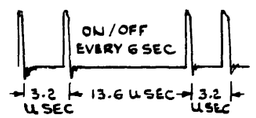
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U78-7		2.4 to 5.2 VDC level
		U54-8		0 VDC
		U43-8		0 VDC
		U53-8		

Table 6-33. Mag Tape Controller PC Card A1A3A14, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U50-13		2.4 to 5.2 VDC level
		U5-8		2.4 to 5.2 VDC level
		U6-6		Same as U49-9
13			Rewind and remove ATP tape.	
14			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
15			Disconnect edge-connector from Mag Tape Controller PC card A1A3A14.	

Table 6-33. Mag Tape Controller PC Card A1A3A14, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
16			Remove Mag Tape Controller PC Card A1A3A14 from card extender.	
17			Reinstall Mag Tape Controller PC card A1A3A14 in Processor.	
18			Connect edge-connector to Mag Tape Controller PC card A1A3A14.	
19			Close Program Maintenance Panel.	
20			Secure bezel to Processor with four screws.	

m. Type in:

3 (C/R)

n. The TTY shall print out:

DRIVES =

o. Type in:

1(C/R)

p. The TTY shall print out:

UNIT =

q. Type in:

0(C/R)

p. The TTY shall print out:

RD/WRT or WRT (1 or 0) =

s. Type in:

1(C/R)

t. The TTY shall print out:

SET DRV SLCT UNIT 0 = 0,
UNIT 1 = 1, ETC, PRS RUN

u. Depress RUN.

V. The TTY shall print out:

DFN TST PRMTRS (1 or 0) =

W. Type in:

0(C/R)

x. The TTY shall print out:

RCDS =

y. Type in:

5(C/R)

z. The TTY shall print out:

WRDS =

aa. Type in:

2O(C/R)

ab. The TTY shall print out:

DATA =

ac. Type in:

5599(C/R)

ad. The TTY shall print out:

RWND & LV ALL UNITS ON LINE,
LOAD, WRT EN, PRS RUN

ae. Remove ATP tape from Mag Tape Unit 1.

af. Load a blank tape (with a write enable ring) on Mag Tape Unit 1 as described in preceding steps c and d.

ag. On Program Maintenance Panel:

1. Enter hexidecimal 100 in address line.

2. Enter hexidecimal 4004 in data line.

ah. Depress run switch.

ai. The TTY shall print out the following:

TST 01
** UNIT 0
TST 02
TST 03

aj. When TST 03 starts, immediately press write switch in ADDRESS line.

ak. TST 03 loops.

al. Go to step 9 of table 6-33.

6-66. BLOCK TRANSFER ADAPTER PC CARD COMPONENT PERFORMANCE TEST. The component performance test for the Block Transfer Adapter PC card is used to isolate malfunctions to an IC or group of IC's. To accomplish the Block Transfer Adapter PC

card component performance test perform the procedure in table 6-34.

6-67. After step 5 of table 6-34, load the ATP test tape as follows:

a. Open Program Maintenance Panel.

b. On Processor Auto-Load PC card A1A3A9, set the four red toggle switches, designated from top to bottom as S1 through S4, as follows: S1 and S2 to up position, S3 and S4 to down position.

Mount and thread ATP tape on Mag Tape Unit 1 (A1A1).

d. On Mag Tape Unit, perform the following:

1. Press LOAD switch.

2. When tape movement stops press LOAD switch again.

3. When LOAD lamp is lighted, press ON LINE switch.

4. If LOAD lamp is not lighted after the tape reel has made five or more revolutions, press REWIND switch; then, when LOAD lamp lights, press ON LINE switch.

e. Press reset and load switch.

f. When tape motion stops repeat step e twelve more times, to reach the thirteenth program (tape motion must come to a stop after each load).

g. Press run switch.

h. The TTY shall print out:

SUE MAG TAPE (BTA) TP

R/R ORC (1 or O)=

i. Type in:

1(C/R)

j. The TTY shall print out:

ADDR =

k. Type in:

F8CO(C/R)

1. The TTY shall print out:

L V L =

m. Type in:

3(C/R)

n. The TTY shall print out:

DRIVES =

0. Type in:

1(C/R)

p. The TTY shall print out:

UNIT =

q. Type in:

0(C/R)

r. The TTY shall print out:

RD/WRT or WRT (1 or 0) =

S. Type in:

1(C/R)

t. The TTY shall print out:

SET DRV SLCT UNIT 0 = 0,
UNIT 1 = 1, ETC, PRS RUN

u. Depress run switch.

v. The TTY shall print out:

DFN TST PRMTRS (1 or 0) =

Table 6-34. Block Transfer Adapter PC Card A1A3A13, Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
2			Remove four screws that secure bezel to Processor.	
3			Open Program Maintenance Panel.	
4			Place Block Transfer Adapter PC card A1A3A13 on card extender.	
5			Set AC POWER 120V switch on Multiple Power Supply 1 to ON. Press POWER ALARM RESET switch on.	
6			For instructions to load program tape see paragraph 6-67.	
7	Sequentially connect oscilloscope to test point and adjust to display indicated waveform.	U3-9		

Table 6-34. Block Transfer Adapter PC Card A1A3A13, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U36-8		
		U26-6		2.4 to 5.2 VDC level
		U36-12		2.4 to 5.2 VDC level
		U15-2		2.4 to 5.2 VDC level

Table 6-34. Block Transfer Adapter PC Card A1A3A13, Performance Test (cont)

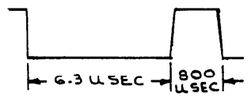
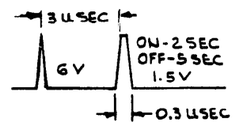
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U7-6		
		U5-8		
		U4-8		0 VDC
		U46-2		2.4 to 5.2 VDC

Table 6-34. Block Transfer Adapter PC Card A1A3A13, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U45-3		2.4 to 5.2 VDC
		U29-11		2.4 to 5.2 VDC
		U24-5		2.4 to 5.2 VDC
		U57-3		0 VDC

Table 6-34. Block Transfer Adapter PC Card A1A3Al3, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U48-8		2.4 to 5.2 VDC
		U48-6		2.4 to 5.2 VDC
		U57-8		2.4 to 5.2 VDC
		U40-8		2.4 to 5.2 VDC

Table 6-34. Block Transfer Adapter PC Card A1A3A13, Performance Test (cont)

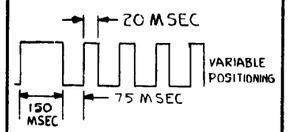
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U13-8		2.4 to 5.2 VDC
		U42-9		
		U15-6		0 VDC
		U32-6		0 VDC

Table 6-34. Block Transfer Adapter PC Card A1A3A13, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		P1-B33		5 VDC level
		U33-8		2.4 to 5.2 VDC level
		U32-8		2.4 to 5.2 VDC level
		U44-8		2.4 to 5.2 VDC level

Table 6-34. Block Transfer Adapter PC Card A1A3A13, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U51-10		Same as U42-9 inverted
		U51-8		2.4 to 5.2 VDC at 2 sec intervals
		U74-2		Same as U42-9
		U74-8		Same as U51-10

Table 6-34. Block Transfer Adapter PC Card A1A3A13, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U51-2		2.4 to 5.2 VDC level
		U51-4		2.4 to 5.2 VDC level
		U51-6		2.4 to 5.2 VDC level
		U72-4		2.4 to 5.2 VDC level

Table 6-34. Block Transfer Adapter PC Card A1A3A13, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U72-6		2.4 to 5.2 VDC level
		U55-12		2.4 to 5.2 VDC level
		U55-2		2.4 to 5.2 VDC level
		U74-12		2.4 to 5.2 VDC level

Table 6-34. Block Transfer Adapter PC Card A1A3A13, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U74-10		0 VDC
		U74-4		2.4 to 5.2 VDC level
		U78-4		2.4 to 5.2 VDC level
		U75-8		2.4 to 5.2 VDC level

Table 6-34. Block Transfer Adapter PC Card A1A3A13, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U61-6		Same as U51-10
		U61-10		2.4 to 5.2 VDC level
		U61-4		Same as U51-10
		U61-2		Same as U51-10

Table 6-34. Block Transfer Adapter PC Card A1A3A13, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U72-10		Same as U51-10
		U72-12		Same as U51-10
		U72-8		2.4 to 5.2 VDC level
		U72-2		2.4 to 5.2 VDC level

Table 6-34. Block Transfer Adapter PC Card A1A3A13, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U55-8		2.4 to 5.2 VDC level
		U55-10		2.4 to 5.2 VDC level
		U55-4		2.4 to 5.2 VDC level
		U55-6		2.4 to 5.2 VDC level

Table 6-34. Block Transfer Adapter PC Card A1A3A13, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U78-10		2.4 to 5.2 VDC level
		U78-12		2.4 to 5.2 VDC level
		U78-8		2.4 to 5.2 VDC level
		U78-2		2.4 to 5.2 VDC level

Table 6-34. Block Transfer Adapter PC Card A1A3A13, Performance Test (cont)

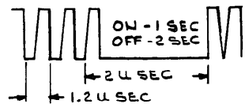
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U75-6		Same as U42-9
		U66-9		Same as U51-10
		U66-7		2.4 to 5.2 VDC level
		U67-7		

Table 6-34. Block Transfer Adapter PC Card A1A3A13, Performance Test (cont)

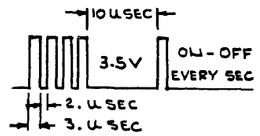
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U67-9		
		U68-12		
		U68-9		Same as U68-12
		U68-4		2.4 to 5.2 VDC level

Table 6-34. Block Transfer Adapter PC Card A1A3A13, Performance Test (cont)

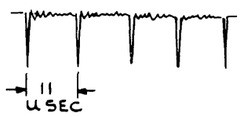
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U68-7		2.4 to 5.2 VDC level
		U56-9		2.4 to 5.2 VDC level
		U56-12		
		U56-7		2.4 to 5.2 VDC level

Table 6-34. Block Transfer Adapter PC Card A1A3A13, Performance Test (cont)

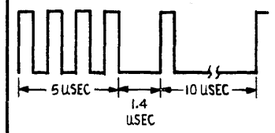
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U56-4		2.4 to 5.2 VDC level
		U79-12		2.4 to 5.2 VDC level
		U79-9		
		U79-4		2.4 to 5.2 VDC level

Table 6-34. Block Transfer Adapter PC Card A1A3A13, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U79-7		2.4 to 5.2 VDC level
		U26-8		2.4 to 5.2 VDC level
8			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
9			Remove Block Transfer Adapter PC card A1A3A13 from card extender.	
10			Reinstall Block Transfer Adapter PC card A1A3A13 in Processor.	
11			Close Program Maintenance.	
12			Secure bezel to Processor with four screws.	

w. Type in:

0(C/R)

x. The TTY shall print out:

RCDS =

y. Type in:

S(C/R).

2. The TTY shall print out:

WRDS =

aa. Type in:

20(C/R)

ab. The TTY shall print out:

DATA =

ac. Type in:

5599(C/R)

ad. The TTY shall print out:

RWND & LV ALL UNITS ON LINE,
LOAD, WRT EN, PRS RUN

ae. Remove ATP tape from Mag Tape Unit 1.

af. Load a blank tape (with a write enable ring) on Mag Tape Unit 1 as described in preceding steps c and d.

ag. On program maintenance panel:

1. Enter hexidecimal 100 in address line.

2. Enter hexidecimal 4004 in data line.

ah. Depress run switch.

ai. The TTY shall print out the following:

TST 01
** UNIT 0
TST 02
TST 03
TST 04
TST 05
TST 06
TST 07

aj. When TST 07 starts, immediately press write switch in address line.

ak. TST 07 loops.

al. Go to step 7 of table 6-34.

6-68. I/O CONTROLLER PC CARD COMPONENT PERFORMANCE TEST (SWITCH GROUP ONLY). The component performance test for the I/O Controller PC card is employed to isolate malfunctions to an IC or group of IC'S. To accomplish the I/O Controller PC card component performance test perform the procedure in table 6-35.

6-69. After step 9 of table 6-35 connect SIT box, load SSGP, and perform operational test as described in T.O. 33D7-50-125-1. When operational test is complete, TTY prints out:

INITIAL RUN COMPLETE

NEXT TEST =

a. Type in:

LCCLA(C/R)

b. TTY will printout:

PT =

C. Type in:

N(C/R)

d. CCLA test will now loop.

e. Go to step 11 of table 6-35.

6-70. PARALLEL I/O PC CARD COMPONENT PERFORMANCE TEST. The component performance test for the Parallel I/O PC card is used to isolate malfunctions to an IC or group of IC's. To accomplish the Parallel

Table 6-35. I/O Controller PC Card A1A3A15, Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
2			Remove four screws that secure bezel to Processor.	
3			Open Program Maintenance Panel.	
4			Disconnect interface plug from front of Processor PC Cards A1A3A15 through A1A3A19. Remove I/O Control PC Card A1A3A15 and Modem Control PC Card A1A3A12.	
5			Insert PC Card extender into slot A1A3A12. Place I/O Control PC Card on extender.	
6			Insert PC Card extender (STELMA Part No. 80331730) into slot A1A3A15. Connect plug from extender to front of I/O Control PC Card.	
7			Reconnect interface plug on front of PC Card A1A3A15 through A1A3A19.	
8			Set AC POWER 120V switch on Multiple Power Supply 1 to ON.	
9			On Alarm and Control Panel, press POWER ALARM RESET switch.	

Table 6-35. I/O Controller PC Card A1A3A15, Performance Test (cont)

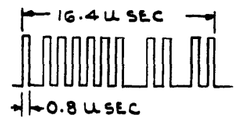
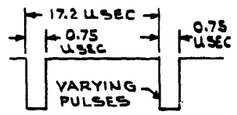
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
10			For instructions to load program tape, see paragraph 6-69.	
11	Sequentially connect oscilloscope to test points and adjust to observe indicated waveform.	U33-6		
		U21-1		
		U21-3		
		U21-5		Same as U21-3

Table 6-35. I/O Controller PC Card A1A3A15, Performance Test (cont)

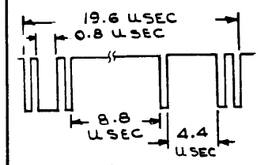
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U21-7		Same as U21-3
		U22-5		
		U73-2		2.4 to 5.2 VDC
		U45-11		0 VDC

Table 6-35. I/O Controller PC Card A1A3A15, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U60-3		0 VDC
		U60-6		0 VDC
		U27-12		
		U56-12		2.4 to 5.2 VDC

Table 6-35. I/O Controller PC Card A1A3F15, Performance Test (cont)

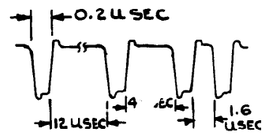
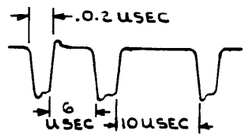
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U1-8		
		U56-2		2.4 to 5.2 VDC
		U19-2		
		U56-10		2.4 to 5.2 VDC

Table 6-35. I/O Controller PC Card A1A3A15, Performance Test (cont)

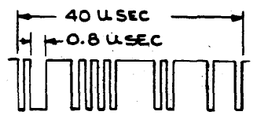
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U58-12		0 VDC
		U31-11		
		U71-7		2.4 to 5.2 VDC
		U77-12		2.4 to 5.2 VDC

Table 6-35. I/O Controller PC Card A1A3A15, Performance Test (cont)

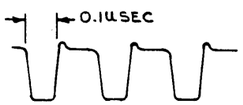
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U42-1		
		U68-6		2.4 to 5.2 VDC
		U90-8		2.4 to 5.2 VDC
		U90-6		2.4 to 5.2 VDC

Table 6-35. I/O Controller PC Card A1A3A15, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U50-8		2.4 to 5.2 VDC
		U63-11		0 VDC
		U49-6		2.4 to 5.2 VDC
		U29-8		0 VDC

Table 6-35. I/O Controller PC Card A1A3A15, Performance Test (cont)

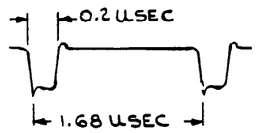
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U63-6		2.4 to 5.2 VDC
		U4-4		
		U4-6		Same as U4-4
		U4-8		Same as U4-4

Table 6-35. I/O Controller PC Card A1A3A15, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U4-10		Same as U4-4
		U1-10		+15 VDC
		U16-6		0 VDC
		U30-8		0 VDC

Table 6-35. I/O Controller PC Card A1A3A15, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U28-10		2.4 to 5.2 VDC
		U28-13		0 VDC
		U28-1		0 VDC
		U28-4		0 VDC

Table 6-35. I/O Controller PC Card A1A3A15, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U42-10		0 VDC
		U48-8		2.4 to 5.2 VDC level
		U17-8		2.4 to 5.2 VDC
		U31-3		2.4 to 5.2 VDC

Table 6-35. I/O Controller PC Card A1A3A15, Performance Teat (cont)

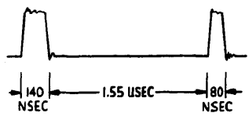
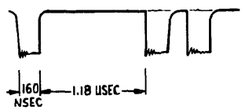
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U53-8		2.4 to 5.2 VDC
		U37-6		
		U75-8		
		U59-11		2.4 to 5.2 VDC level

Table 6-35. I/O Controller PC Card A1A3P15, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U2-8		2.4 to 5.2 VDC level
		U2-6		2.4 to 5.2 VDC level
		U2-4		2.4 to 5.2 VDC level
		U56-8		2.4 to 5.2 VDC level

Table 6-35. I/O Controller PC Card A1A3A15, Performance Test (cont)

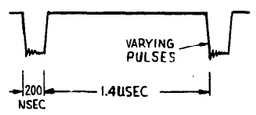
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U56-4		2.4 to 5.2 VDC level
		U34-11		2.4 to 5.2 VDC level
		U33-11		
		U27-8		2.4 to 5.2 VDC level

Table 6-35. I/O Controller PC Card A1A3A15, Performance Test (cont)

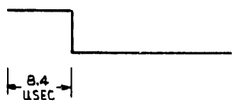
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U8-4		0 VDC
		U53-2		2.4 to 5.2 VDC level
		U80-8		
		U73-6		Same as U33-11

Table 6-35. I/O Controller PC Card A1A3A15, Performance Test (cont)

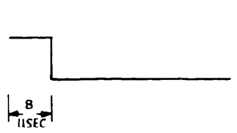
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U80-6		2.4 to 5.2 VDC level
		U36-2		0 VDC
		U44-6		Same as U33-11
		XA1-B37 U56-6		

Table 6-35. I/O Controller PC Card A1A3A15, Performance Test (cont)

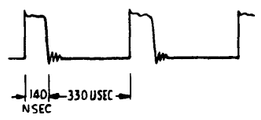
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U43-8		2.4 to 5.2 VDC level
		U54-4		
		U54-6		Same as U54-4
		U54-8		Same as U54-4

Table 6-35. I/O Controller PC Card A1A3A15, Performance Test (cont)

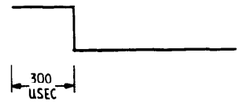
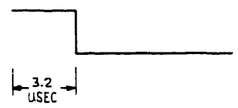
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U27-2		
		U27-4		Same as U27-2
		U80-12		
		U79-4		Same as U80-12

Table 6-35. I/O Controller PC Card A1A3A15, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U53-4		0 VDC
		U79-12		0 VDC
		U40-4		0 VDC
		U40-12		0 VDC

Table 6-35. I/O Controller PC Card A1A3A15, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
12			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
13			Disconnect edge-connector from I/O Controller PC card.	
14			Remove I/O Controller PC card from card extender and remove card extender.	
15			Disconnect interface plug from PC cards A1A3A15 through A1A3A19. Remove card extender (STELMA Part No. 80331730).	
16			Reinstall I/O Controller PC card A1A3A15 and Modem Control PC card A1A3A12 in Processor.	
17			Reconnect interface plug to PC cards A1A3A15 through A1A3A19.	
18			Close Program Maintenance Panel.	
19			Secure bezel to Processor with four screws.	

I/O PC card component performance test perform the procedure in table 6-36.

6-71. MODEM CONTROLLER 1 PC CARD COMPONENT PERFORMANCE TEST. The component performance test for the Modem Controller 1 PC card is used to isolate malfunctions to an IC or group of IC'S. To accomplish the Modem Controller 1 PC card component performance test perform the procedure in table 6-3 7.

6-72. After step 7 of table 6-37, load the ATP test tape as follows:

a. Open Program Maintenance Panel.

b. On Processor Auto-Load PC card A1A3A9, set the four red toggle switches, designated from top to bottom as S1 through S4, as follows: S1 and S2 to up position, S3 and S4 to down position.

Mount and thread ATP tape on Mag Tape Unit 1 (A1A1).

d. On Mag Tape Unit, perform the following:

1. Press LOAD switch.

2. When tape movement stops press LOAD switch again.

3. When LOAD lamp is lighted, press ON LINE switch.

4. If LOAD lamp is not lighted after the tape reel has made five or more revolutions, press REWIND switch; then, when LOAD lamp lights, press ON LINE switch.

e. Press reset and load switch.

f. When tape motion stops, repeat step e eleven more times, to reach the twelfth program. (Tape motion must come to a stop after each load.)

g. Press run switch.

h. The TTY shall print out:

TTY TEST

TTY LEV =

i. Type in:

2(C/R).

j. The TTY shall print out:

TTY ADD =

k. Type in either:

F930(C/R) for Switch Group

F940(C/R) for ACOC Group

1. The TTY shall print out:

BTA = (YES = l, NO = O)

m. On Program Maintenance Panel:

1. Enter hexidecimal 100 in address line.

2. Enter hexidecimal 4004 in data line.

n. Type in:

O(C/R)

o. The TTY shall print out:

TST 01

p. When TST 01 starts, immediately press write switch in address line.

q. Go to step 9 of table 6-37.

6-73. PRINTER CONTROLLER PC CARD COMPONENT PERFORMANCE TEST (ACOC GROUP ONLY). The component performance test for the Printer Controller PC card is used to isolate malfunctions to an IC or group of IC's. To accomplish the Printer Controller PC card component performance test perform the procedure in table 6-38.

6-74. After step 7 of table G-38, load the ATP test tape as follows:

a. Open Program Maintenance Panel.

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
2			Remove four screws that secure bezel to Processor.	
3			Open Program Maintenance Panel.	
4			Remove edge-connector from Parallel I/O PC card A1A3A10.	
5			Place Parallel I/O PC card A1A3A10 on card extender.	
6			Connect edge-connector to Parallel I/O PC card A1A3A10.	
7			Set AC POWER 120V switch on Multiple Power Supply to ON.	
8			Load and run site program tape as described in T.O. 31W2-2G-271 or T.O. 31W2-2G-281, as applicable.	
9	Sequentially connect multimeter to test points and adjust to indicate 5 volts dc.	U9-4		Observe that multimeter indicates voltage level between 2.4 volts dc and 5.2 volts dc at all test points.

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U27-10		
		U27-4		
10	Sequentially connect multimeter to test points and adjust to indicate 0 volt dc.	U9-2		Observe that multimeter indicates voltage level between 0.0 volt dc and 0.4 volt dc at all test points.
		U9-6		
		U27-8		

Table 6-36. Parallel I/O PC Card *A1A3A10*, Performance Test (cont)

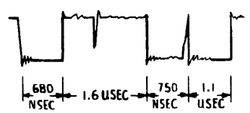
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U27-12		
		U27-6		
11	Sequentially connect oscilloscope to test point and adjust to display indicated waveform.	U18-5		0 VDC
		U8-8		

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test (cont)

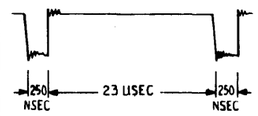
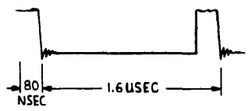
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U7-8		
		U7-6		2.4 to 5.2 VDC level
		U3-8		
		U17-8		0 VDC

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test (cont)

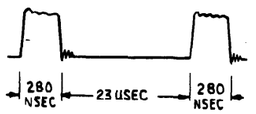
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U17-11		
		U64-8		2.4 to 5.2 VDC level
		J2-A17		2.4 to 5.2 VDC level
		J2-A16		2.4 to 5.2 VDC level

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U2-A15		0 VDC
		J2-A13		2.4 to 5.2 VDC level
		J2-A12		0 VDC
		J2-A11		2.4 to 5.2 VDC level

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J2-A10		0 VDC
		E14		0 VDC
		E15		0 VDC
		E40		2.4 to 5.2 VDC level

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		E39		0 VDC
		E41		0 VDC
		E42		0 VDC
		E43		0 VDC

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		E44		0 VDC
		U65-6		0 VDC
		U74-8		0 VDC
		U65-4		2.4 to 5.2 VDC level

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U65-12		2.4 to 5.2 VDC level
		U65-10		2.4 to 5.2 VDC level
		U65-8		2.4 to 5.2 VDC level
		U69-2		2.4 to 5.2 VDC level

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		E13		0 VDC
		J2-A7		2.4 to 5.2 VDC level
		U15-6		2.4 to 5.2 VDC level
		E2		2.4 to 5.2 VDC level

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U13-8		2.4 to 5.2 VDC level
		U31-8		0 VDC
		U31-6		2.4 to 5.2 VDC level
		U27-2		2.4 to 5.2 VDC level

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		J2-A5		2.4 to 5.2 VDC level
		J2-A6		2.4 to 5.2 VDC level
		U2-4		2.4 to 5.2 VDC level
		U42-13		0 VDC

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U33-3		0 VDC
		U36-6		2.4 to 5.2 VDC level
		U49-7		0 VDC
		U49-9		0 VDC

Table 6-36. Parallel Parallel I/O PC Card A1A3A10, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U33-3		0 VDC
		U36-6		2.4 to 5.2 VDC level
		U49-7		0 VDC
		U49-9		0 VDC

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U33-3		0 VDC
		U36-6		2.4 to 5.2 VDC level
		U49-7		0 VDC
		U49-9		0 VDC

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test (cont)

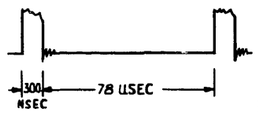
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U48-9		
		U48-7		Same as U48-9
		U59-9		2.4 to 5.2 VDC
		U59-7		2.4 to 5.2 VDC

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U58-9		2.4 to 5.2 VDC
		U58-7		2.4 to 5.2 VDC level
		U68-4		2.4 to 5.2 VDC level
		U68-7		2.4 to 5.2 VDC level

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U68-12		0 VDC
		U68-9		0 VDC
		U78-9		0 VDC
		U78-12		0 VDC

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U78-4		0 VDC
		U78-7		0 VDC
		U54-8		0 VDC
		U43-8		0 VDC

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U53-8		0 VDC
		U50-13		2.4 to 5.2 VDC level
		U5-8		2.4 to 5.2 VDC level
		U6-6		2.4 to 5.2 VDC level

Table 6-36. Parallel I/O PC Card A1A3A10, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
12			Rewind and remove site program tape.	
13			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
14			Disconnect edge-connector from Parallel I/O PC card A1A3A10.	
15			Remove Parallel I/O PC card A1A3A10 from extender.	
16			Reinstall Parallel I/O PC card A1A3A10 in Processor.	
17			Connect edge-connector to Parallel I/O PC card A1A3A10.	
18			Close Program Maintenance Panel.	
19			Secure bezel to Processor with four screws.	

Table 6-37. Modem Controller 1 PC Card A1A3A12, Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
2			Remove four screws that secure bezel to Processor.	
3			Open Program Maintenance Panel SWB open.	
4			Remove edge-connector from Modem Controller 1 PC card A1A3A12.	
5			Place Modem Controller 1 PC card A1A3A12 on card extender.	
6			Connect edge-connector to Modom Controller 1 PC card A1A3A12.	
7			Set AC POWER 120V switch on Multiple Power Supply 1 to ON. Press POWER ALARM RESET switch on Alarm and Control Panel.	
8			For Instructions to Load ATP tape see paragraph 6-72.	
9	Connect multimeter to test point and adjust to observe -12 volts dc level.	Q1-E		Observe that voltage level is -12 volts ± 2 volts.

Table 6-37. Modem Controller 1 PC Card A1A3A12, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
10	Connect multimeter to test point and adjust to observe 12 volts dc level.	Q2-E		Observe the voltage level is +12 volts ±2 volts.
11	Sequentially connect multimeter to observe test point and adjust to 5 volts dc level.	U38-2		Observe that voltage level is 2.4 to 5.2 VDC at all test points.
		U38-8		
		U50-12		

Table 6-37. Modem Controller 1 PC Card A1A3A12, Performance Test (cont)

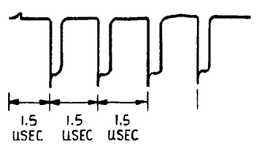
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U50-10		
12	Connect multimeter to test point and adjust to observe 0 volt dc level.	U38-10		Observe that voltage level is between 0.0 volt dc and 0.4 volt dc at all test points
		U38-12		
		U50-6		

Table 6-37. Modem Controller 1 PC Card A1A3A12, Performance Test (cont)

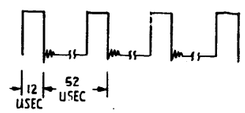
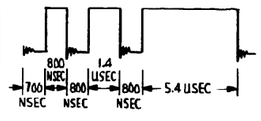
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U50-8		
13	Sequentially connect oscilloscope to test point and adjust to observe indicated waveform	U61-3		
		U36-9		0 VDC
		U2-8		

Table 6-37. Modem Controller 1 PC Card A1A3A12, Performance Test (cont)

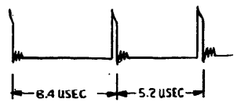
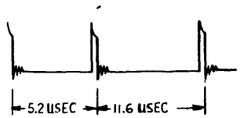
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U1-8		0 VDC
		U4-12		
		U4-4		
		U55-6		Same as U4-4

Table 6-37. Modem Controller 1 PC Card A1A3A12, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U55-3		Same as U4-12
		U34-12		0 VDC
		U24-8		2.4 to 5.2 VDC level
		U33-8		2.4 to 5.2 VDC level

Table 6-37. Modem Controller 1 PC Card A1A3A12, Performance Test **(cont)**

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U61-5		2.4 to 5.2 VDC level
		U36-6		2.4 to 5.2 VDC level
		U33-11		2.4 to 5.2 VDC level
		U35-8		0 VDC

Table 6-37. Modem Controller 1 PC Card A1A3A12, Performance Test (cont)

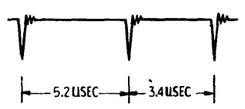
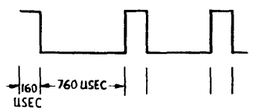
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U26-12		
		U48-6		
		U48-3		Same as U48-6
		U4-2		2.4 to 5.2 VDC

Table 6-37. Modem Controller 1 PC Card A1A3A12, Performance Test (cont)

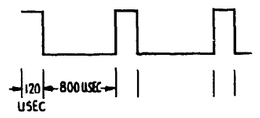
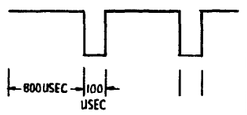
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U4-10		
		U68-6		
		U68-8		Same as U48-6
		U22-4		0 VDC

Table 6-37. Modem Controller 1 PC Card A1A3A12, Performance Test (cont)

OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
	U21-6		0 VDC
	U21-8		0 VDC
	U53-14		2.4 to 5.2 VDC level
	U41-11		2.4 to 5.2 VDC level

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NAVELEX 0967-464-0010

Table 6-37. Modem Controller 1 PC Card A1A3A12, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U51-6		2.4 to 5.2 VDC level
		U32-8		2.4 to 5.2 VDC level
		U41-6		2.4 to 5.2 VDC level
		U57-8		2.4 to 5.2 VDC level

Table 6-37. Modem Controller 1 PC Card A1A3A12, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U77-20		2.4 to 5.2 VDC level
		U77-18		2.4 to 5.2 VDC level
		U77-16		2.4 to 5.2 VDC level
		U77-14		2.4 to 5.2 VDC level

Table 6-37. Modem Controller 1 PC Card A1A3A12, Performance Test (cont)

STEP	OPERATION OF TEST . EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U77-10		2.4 to 5.2 VDC level
		U77-8		2.4 to 5.2 VDC level
		U77-6		2.4 to 5.2 VDC level
		U77-4		2.4 to 52. VDC level

Table 6-37. Modem Controller 1 PC Card A1A3A12, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U66-6		0 VDC
		J1-A5		-9 VDC
		J1-B7		+15 VDC
		J1-B3		+15 VDC

Table 6-37. Modem Controller 1 PC Card A1A3A12, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U23-3		0 VDC
		U16-8		0 VDC
		U16-3		2.4 to 5 VDC level
		U15-6		0 VDC

Table 6-37. Modem Controller 1 PC Card A1A3A12, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U25-8		2.4 to 5 VDC level
		U15-8		2.4 to 5 VDC level
		U78-9		2.4 to 5 VDC level
		U78-7		2.4 to 5 VDC level

Table 6-37. Modem Controller 1 PC Card A1A3A12, Performance Test (cont)

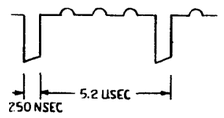
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U67-9		2.4 to 5 VDC level
		U67-7		2.4 to 5.2 VDC level
		U58-9		
		U58-7		Same as U58-9

Table 6-37. Modem Controller 1 PC Card A1A3A12, Performance Test (cont)

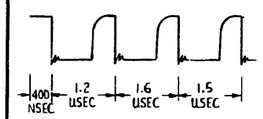
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U56-9		Same as U58-9
		U56-7		Same as U58-9
		U29-12		
		U40-2		2.4 to 5.2 VDC level

Table 6-37. Modem Controller 1 PC Card A1A3A12, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
14			Rewind and remove ATP tape.	
15			Set AC POWER 120 V switch on Multiple Power Supply 1 to OFF.	
16			Disconnect edge-connector from Modem Controller 1 PC card A1A3A12.	
17			Remove Modem Controller 1 PC card A1A3A12 from card extender.	
18			Reinstall Modem Controller 1 PC card A1A3A12 in Processor.	
19			Connect edge-connector to Modem Controller 1 PC card A1A3A12.	
20			Close Program Maintenance Panel.	
21			Secure bezel to Processor with four screws.	

Table 6-38. Printer Controller PC Card A1A3A16, Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 1 TO OFF.	
2			Remove four screws that secure bezel to Processor.	
3			Open Program Maintenance Panel.	
4			Remove edge-connector from Printer Controller PC card A1A3A16.	
5			Place Printer Controller PC card A1A3A16 on card extender.	
6			Connect edge-connector to Printer Controller PC card A1A3A16.	
7			Set AC POWER 120V switch on Multiple Power Supply 1 to ON. Press POWER ALARM RESET switch on Alarm and Control Panel.	
8			For instructions to load ATP tape see paragraph 6-74.	
9	Connect multimeter to test point and adjust to observe -12 volts dc level.	Q1-E		Observe that voltage level is -12 VDC ±2 volts.

Table 6-38. Printer Controller PC Card A1A3A16, Performance Test (cont)

OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
To test point and adjust to observe 12 volts dc level.	Q2-E		Observe that voltage level is +12 VDC ±2V 12+ volts dc.
Sequentially connect multimeter to test point and adjust to observe 5 volts dc level.	U38-12		Observe that voltage level is between 2.4 volts dc and 5.2 volts dc at all test points.
	U38-2		
	U38-8		

Table 6-38. Printer Controller PC Card A1A3A16, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U50-6		
		U50-12		
		U50-10		
12	Connect multimeter to test point and adjust to observe	U38-10		Observe that voltage level is between 0.0

Table 6-38. Printer Controller PC Card A1A3A16, Performance Test (cont)

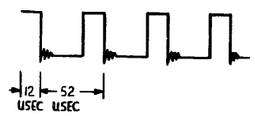
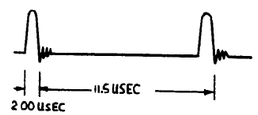
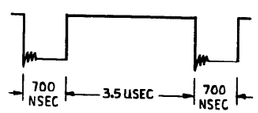
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U50-8		
13	Sequentially connect oscilloscope to test point and adjust to observe indicated waveform.	U61-3		
		U36-9		
		U2-8		

Table 6-38. Printer Controller PC Card A1A3A16, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U1-8		0 VDC
		U4-12		
		U4-4		0 VDC
		U55-6		0 VDC

Table 6-38. Printer Controller PC Card A1A3A16, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U58-3		Same as U4-12
		U34-12		0 VDC
		U24-8		2.4 to 5.2 VDC
		U33-8		Same as U24-8

Table 6-38. Printer Controller PC Card A1A3A16, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U61-6		2.4 to 5.2 VDC level
		U36-6		2.2 to 5.2 VDC level
		U33-11		0 VDC
		U35-8		Same as U4-12

Table 6-38. Printer Controller PC Card A1A3A16, Performance Test (cont)

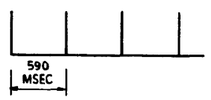
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U26-12		Reverse of U4-12
		U48-6		2.4 to 5.2 VDC level
		U48-3		2.4 to 5.2 VDC level
		U4-2		

Table 6-38. Printer Controller PC Card A1A3A16, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U4-10		Reverse of U4-2
		U68-6		Same as U4-2
		U68-8		Same as U4-2
		U22-4		2.4 to 5.2 VDC level

Table 6-38. Printer Controller PC Card A1A3A16, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U21-6		0 VDC
		U21-8		0 VDC
		U53-14		2.4 to 5.2 VDC level
		U41-11		2.4 to 5.2 VDC level

Table 6-38. Printer Controller PC Card A1A3A16, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U21-6		0 VDC
		U21-8		0 VDC
		U53-14		2.4 to 5.2 VDC level
		U41-11		2.4 to 5.2 VDC level

Table 6-38. Printer Controller PC Card A1A3Al6, Performance Test (Cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U51-6		2.4 to 5.2 VDC level
		U32-8		2.4 to 5.2 VDC level
		U41-6		2.4 to 5.2 VDC level
		U57-8		2.4 to 5.2 VDC level

Table 6-38. Printer Controller PC Card A1A3A16, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U77-20		0 VDC
		U77-18		0 VDC
		U77-16		2.4 to 5.2 VDC level
		U77-14		0 VDC

Table 6-38. Printer Controller PC Card A1A3A16, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U77-10		0 VDC
		U77-8		0 VDC
		U77-6		0 VDC
		U77-4		0 VDC

Table 6-38. Printer Controller PC Card A1A3A16, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U66-6		0 VDC
		J1-A5		-8 VDC
		J1-B7		+15 VDC
		J1-B3		+15 VDC

Table 6-38. Printer Controller PC Card A1A3A16, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U23-3		2.4 to 5.2 VDC level
		U16-8		2.4 to 5.2 VDC level
		U16-3		0 VDC
		U15-6		0 VDC

Table 6-38. Printer Controller PC Card A1A3A16, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U25-8		2.4 to 5.2 VDC level
		U15-8		2.4 to 5.2 VDC level
		U78-9		Same as U4-12
		U78-7		Same as U4-12

Table 6-38. Printer Controller PC Card A1A3A16, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U67-9		Same as U4-12
		U67-7		Same As U4-12
		U58-9		Same as U4-12
		U58-7		Same as U4-12

Table 6-38. Printer Controller PC Card A1A3A16, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U56-9		Same as U4-12
		U56-7		0 VDC
		U29-12		Same as U4-12
		U40-2		0 VDC

Table 6-38. Printer Controller PC Card A1A3A16, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
14			Rewind and remove ATP tape.	
15			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
16			Disconnect edge-connector from Printer Controller PC card A1A3A16.	
17			Remove Printer Controller PC card A1A3A16 from card extender.	
18			Reinstall Printer Controller PC card A1A3A16 in Processor.	
19			Connect edge-connector to Printer Controller PC card A1A3A16.	
20			Close Program Maintenance Panel.	
21			Secure bezel to Processor with four screws.	

b. On Processor Auto-Load PC card A1A3A9, set the four red toggle switches, designated from top to bottom as S1 through S4, as follows: S1 and S2 to up position, S3 and S4 to down position.

Mount and thread ATP tape on Mag Tape Unit 1 (A1A1).

d. On Nag Tape Unit, perform the following:

1. Press LOAD switch.

2. When tape movement stops press LOAD switch again.

3. When LOAD lamp is lighted, press ON LINE switch.

4. If LOAD lamp is not lighted after the tape reel has made five or more revolutions, press REWIND switch; then, when LOAD lamp lights, press ON LINE switch.

e. Press reset and load switch.

f. When tape motion stops, repeat step e eleven more times, to reach the twelfth program. (Tape motion must come to a stop after each load .)

g. Press run switch.

h. The TTY shall print out:

TTY TEST

TTY LEV=

i. Type in:

2 (C / R)

j. The TTY shall print out:

TTY ADD =

k. Type in:

F810(C/R)

1. The TTY shall print out:

BTA = (YES = 1, NO = 0)

m. On Program Maintenance Panel:

1. Enter hexidecimal 100 in address line.

2. Enter hexidecimal 4004 in data line.

n. Type in:

0(C/R)

o. The TTY shall print out:

TST 01

p. When TST 01 starts, immediately press write switch in address line.

q. Go to step 9 of table 6-38.

6-75. MODEM CONTROLLER 2 PC CARD COMPONENT PERFORMANCE TEST (ACOC GROUP ONLY). The component performance test for the Modem Controller 2 PC card is used to isolate malfunctions to an IC or group of IC's. To accomplish the Modem Controller 2 PC card component performance test perform the procedure in table 6-39.

6-76. After step 7 of table 6-39, load the ATP test tape as follows:

a. Remove translucent RFI bezel on front of Processor (A1A3) and open front panel (Program Maintenance Panel).

b. On Processor Auto-Load PC card A1A3A9, set the four red toggle switches, designated from top to bottom as S1 through S4, as follows: S1 and S2 to up position, S3 and S4 to down position.

Mount and thread ATP tape on Mag Tape Unit 1 (A1A1).

d. On Mag Tape Unit, perform the following:

1. Press LOAD switch.

2. When tape movement stops press LOAD switch again.

3. When LOAD lamp is lighted, press ON LINE switch.

4. If LOAD lamp is not lighted after the tape reel has made five or more revolutions, press REWIND switch; then, when LOAD lamp lights, press ON LINE switch.

e. Press reset and load switch.

f. When tape motion stops, repeat step e eleven more times, to reach the twelfth program. (Tape motion must come to a stop after each load.)

g. Press run switch.

h. The TTY shall print out:

TTY TEST

TTY LEV=

i. Type in:

2(C/R

j. The TTY shall print out:

TTY ADD =

k. Type in:

F960(C/R)

1. The TTY shall print out:

BTA = (YES = 1, NO = 0)

m. On Program Maintenance Panel:

1. Enter hexidecimal 100 in ADDR line.

2. Enter hexidecimal 4004 in DATA line.

n. Type in:

0(C/R)

o. The TTY shall print out:

TST 01

p. When TST 01 starts, immediately press write switch in address line.

q. Go to step 9 of table 6-39.

6-77. REPAIR AND REPLACEMENT.

6-78. Repair and replacement consists of repair of Processor and Core Memory PC cards and replacement of PC cards that comprise the Core Memory CM BSM.

6-79. REPAIR. The repair of the Processor and Core Memory is the removal and installation of defective component parts on the PC cards. There are two types of PC cards used in the Processor and Core Memory, standard surface trace and multi-layer cards. Surface trace PC cards are the Core Memory Controller and I/O Controller in the Processor and CM MIA, CM MIB, CM MBA, CM MSA, CM MMA in the Core Memory. Multi-layer PC cards are the CPA, CPB, Bus Controller, Autoload, Parallel I/O, TTY Controller, Modem Controller 1, Block Transfer Adapter, Mag Tape Controller, PBI, PCB, Printer, Controller and Modem Controller 2 in the Processor.

6-80. Surface trace PC card components are removed and installed using standard shop practices. It is not recommended that repair of multi-layer PC cards be attempted by other than highly qualified personnel. Procedures for the removal and installation of axial and multiple lead components on multi-layer PC cards are contained in the following paragraphs.

CAUTION

Only personnel with appropriate experience on similar equipment should attempt the PC card repair procedures given below. If non-qualified personnel attempt repair, irreparable damage to the PC card may result.

CAUTION

Components must be removed and replaced with extreme care to avoid PC card and component damage.

6-81. Axial Lead Components Removal. To remove axial lead components from multi-layer PC cards, proceed as follows:

a. Clip leads on component side of PC card close to surface of PC card.

b. Use a 35 watt soldering iron to remove component leads from circuit side of PC card.

c. Remove excess solder from holes using solder sucker as required.

6-82. Axial Lead Component Installation. To install axial lead components on multi-layer PC cards, proceed as follows:

CAUTION

Ensure that replacement component is properly oriented before soldering to the PC card.

a. Bend the component leads and insert the component into the PC card properly oriented.

b. Solder component leads and turn off excess leads close to PC card.

c. Clean solder connections with isopropyl alcohol.

6-83. Multiple Lead Component Removal. To remove multiple lead components from multi-layer PC cards, proceed as follows:

a. Apply heat to individual leads and remove solder using a solder sucker.

b. Free component leads and remove component from PC card.

c. Check for lifted conductor traces and damage to laminate or components.

6-84. Multiple Lead Component Installation. To install multiple lead components on multi-layer PC cards, proceed as follows:

CAUTION

Ensure that replacement component is properly oriented before soldering to the PC card.

a. Insert properly oriented component into PC card and solder leads.

b. Clean solder connections with isopropyl alcohol.

6-85. REPLACEMENT. The Core Memory CM BSM is comprised of the CM MBA, CM MSA and CM MMA PC cards. Procedures for the replacement of these PC cards are contained in the following CM BSM disassembly and reassembly procedures:

6-86. Disassembly. To disassemble the CM BSM, proceed as follows:

a. Position the CM BSM with the CM MBA PC card on top and remove four screws and fiber washers that secure CM MBA to four jack screw blocks.

b. Remove two screws, lock washers and metal washers at the front edge of the CM MBA that secure CM MBA to CM BSM.

c. Ease the CM MBA PC card off CM BSM and remove the connector on the underside of the CM MBA PC card from the edge-connector on the CM MAA PC card.

CAUTION

Do not remove the core array cover on the CM MMA PC card.

d. Lift the edge-connector of the CM MMA PC card until it is clear of the jack screw blocks.

e. Ease the CM MMA PC card out until the edge-connector of the CM MMA PC card is free from the connector on the CM MSA and then lift the CM MMA clear.

f. Remove four jack screw blocks with fiber washers, metal washers and lock was hers from the CM MSA.

6-87. Reassembly. To reassemble the CM BSM, proceed as follows:

a. Secure fiber washers, metal washers and lock washers with four jack screw blocks to the CM MSA PC card.

b. Place the CM MMA PC card over the CM MSA PC card and ease it on to the CM MSA PC card, fitting it between the four jack screws blocks connecting the CM MMA and CM MSA PC cards edge-connectors.

c. Place the CM MBA PC card over the CM MMA PC card and connect the connector on the underside of the CM MBA PC: card to the edge-connector on the CM MMA PC card.

d. Ease the CM MBA PC card on to the jack screw blocks and secure the CM MBA to the CM BAM with two metal washers, lock washers and screws.

e. Secure CM MBA to four jack screw blocks with four fiber washers and screws.

CAUTION

Ensure all fiber washers are replaced during reassembly to prevent shorts.

f. Check that there are no shorts between the jack screw blocks and ground plane of the CM MMA PC card.

After assembly of the CM BSM, perform the CM MSA, CM MBA, and CM MMA PC card component performance tests.

6-88. TESTING.

6-89. After the repair of any Processor or Core Memory PC card, insert the card in the Switch or ACOC Group, as appropriate, and perform the applicable performance test (see paragraph 6-11).

Table 6-39. Modem Controller 2 PC Card A1A3A17, Performance Test

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
1			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
2			Remove four screws that secure bezel to Processor.	
3			Open Program Maintenance Panel.	
4			Remove edge-connector from Modem Controller 2 PC card A1A3A17.	
5			Place Modem Controller 2 PC card A1A3A17 on card extender.	
6			Connect edge-connector to Modem Controller 2 PC card A1A3A17.	
7			Set AC POWER 120V switch on Multiple Power Supply 1 to ON. Press POWER ALARM RESET switch Alarm and Control Panel.	
8			For instructions to load ATP tape see paragraph 6-76.	
9	Connect multimeter to test point and adjust to observe -12 volts dc level.	Q1-E		Observe that voltage level -12 VDC ±2 volts.

Table 6-39. Modem Controller 2 PC Card A1A3A17, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
10	Connect multimeter to test point and adjust to observe 12 volts dc level.	Q2-E		Observe that voltage level +12 VDC ±2 volts is 12+ volts dc.
11	Sequentially connect multimeter to test point and adjust to observe 5 volts dc level.	U38-10		Observe the voltage level is between 2.4 volts dc and 5.2 volts dc at all test points.
		U38-12		
		U38-8		

Table 6-39. Modem Controller 2 PC Card A1A3A17, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U50-12		
		U50-10		
12	Connect multimeter to test point and adjust to observe 0 volt dc level.	U38-2		Observe that voltage level is between 0.0 volt dc and 0.4 volt dc at all test points.
		U50-6		

Table 6-39. Modem Controller 2 PC Card A1A3A17, Performance Test (cont)

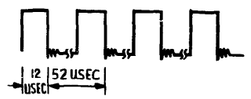
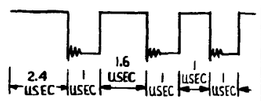
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U50-8		
13	Sequentially connect oscilloscope to test point and adjust to observe indicated waveform.	U61-3		
		U36-9		0 VDC
		U2-8		

Table 6-39. Modem Controller 2 PC Card A1A3A17, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U1-8		0 VDC
		U4-12		0 VDC
		U4-4		0 VDC
		U55-6		0 VDC

Table 6-39. Modem Controller 2 PC Card A1A3A17, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U55-3		0 VDC
		U34-12		0 VDC
		U24-8		2.4 to 5.2 VDC level
		U33-8		2.4 to 5.2 VDC level

Table 6-39. Modem Controller 2 PC Card A1A3A17, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U61-5		2.4 to 5.2 VDC level
		U36-6		2.4 to 5.2 VDC level
		U33-11		2.4 to 5.2 VDC level
		U35-8		0 VDC

Table 6-39. Modem Controller 2 PC Card A1A3A17, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U26-12		2.4 to 5.2 VDC level
		U48-6		2.4 to 5.2 VDC level
		U48-3		2.4 to 5.2 VDC level
		U4-2		0 VDC

Table 6-39. Modem Controller 2 PC Card A1A3A17, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U4-10		0 VDC
		U68-6		0 VDC
		U68-8		2.4 to 5.2 VDC level
		U22-4		2.4 to 5.2 VDC level

Table 6-39. Modem Controller 2 PC Card A1A3A17, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U21-6		0 VDC
		U21-8		0 VDC
		U53-14		2.4 to 5.2 VDC level
		U41-11		2.4 to 5.2 VDC level

Table 6-39. Modem Controller 2 PC Card A1A3A17, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U51-6		2.4 to 5.2 VDC level
		U32-8		2.4 to 5.2 VDC level
		U41-6		2.4 to 5.2 VDC level
		U57-8		2.4 to 5.2 VDC level

Table 6-39. Modem Controller 2 PC Card A1A3A17, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U77-20		0 VDC
		U77-18		0 VDC
		U77-16		0 VDC
		U77-14		0 VDC

Table 6-39. Modem Controller 2 PC Card A1A3A17, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U77-10		0 VDC
		U77-8		0 VDC
		U77-6		0 VDC
		U77-4		0 VDC

Table 6-39. Modem Controller 2 PC Card A1A3A17, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U66-6		0 VDC
		J1-A5		-8 VDC
		J1-B7		+13 VDC
		J1-B3		+13 VDC

Table 6-39. Modem Controller 2 PC Card A1A3A17, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U23-3		2.4 to 5.2 VDC level
		U16-8		0 VDC
		U16-3		2.4 to 5.2 VDC level
		U15-6		0 VDC

Table 6-39. Modem Controller 2 PC Card A1A3A17, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U25-8		2.4 to 5.2 VDC level
		U15-8		2.4 to 5.2 VDC level
		U78-9		0 VDC
		U78-7		0 VDC

Table 6-39. Modem Controller 2 PC Card A1A3A17, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U67-9		0 VDC
		U67-7		0 VDC
		U58-9		0 VDC
		U58-7		0 VDC

Table 6-39. Modem Controller 2 PC Card A1A3A17, Performance Test (cont)

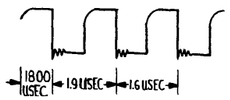
STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
		U56-9		0 VDC
		U56-7		0 VDC
		U29-12		
		U40-2		2.4 to 5.2 VDC level

Table 6-39 1 Modem Controller 2 PC Card A1A3A17, Performance Test (cont)

STEP	OPERATION OF TEST EQUIPMENT	POINT OF TEST	CONTROL SETTINGS AND OPERATION OF EQUIPMENT	PERFORMANCE STANDARDS
14			Rewind and remove ATP tape.	
15			Set AC POWER 120V switch on Multiple Power Supply 1 to OFF.	
16			Disconnect edge-connector from Modem Controller 2 PC card A1A3A17.	
17			Remove Modem Controller 2 PC card A1A3A17 from card extender.	
18			Reinstall Modem Controller 2 PC card A1A3A17 in Processor.	
19			Connect edge-connector to Modem Controller 2 PC card A1A3A17.	
20			Close Program Maintenance Panel.	
21			Secure bezel to Processor with four screws.	

SECTION III

PERFORMANCE TEST CHECKS

6-90. GENERAL.

6-91. The performance test checks, when successfully completed, as sure that Processor and Core Memory functions meet minimum performance standards.

6-92. PRELIMINARY INSTRUCTIONS.

6-93. Prior to the performance test checks perform the following preliminary procedures:

a. Check that all power switches in Data Processing Assembly Al and TTY (KSR-35 at ACOC Group, ASR-35 at Switch Group) are ON.

b. All tests are contained on one ATP test tape; autoload the test tape as described in paragraph 6-15.

6-94. TEST CHECKS.

6-95. Once the preliminary procedures have been accomplished, perform the test checks as described below.

a. Press reset switch and then load switch.

b. When tape motion halts, press run switch.

c. In data line, switch 0 is lit and a loop count is displayed in bits 4 through 15.

d. Repeat steps a. and b.

e. In data line, switch 1 is lit and a loop count is displayed in bits 4 through 15.

f. Repeat steps a. and b.

g. In data line, switches 1 and 0 are tit and a loop count is displayed in bits 4 through 15.

h. Repeat steps a and b.

i. In data line, switch 2 is lit and a loop count is displayed in bits 4 through 15.

j. Press reset switch and then load switch.

k. When tape motion halts, press RUN switch.

1. TTY prints:

INTERRUPT TEST REV A

TST 01

PRESS RUN, OPERATOR ATTENTION

m. Turn OFF LINE FREQ switch (S70) located at lower edge of Program Maintenance Panel.

n. Press run switch and then attn switch.

o. TTY prints:

TST 02

PRESS RUN, OPERATOR ATTENTION

p. Press run switch and then attn switch.

q. TTY prints:

TST 03

PRESS RUN, OPERATOR ATTENTION

r. Press run switch and then attn switch.

s. TTY prints :

TST 04

PRESS RUN, OPERATOR ATTEN-
TION

t. Press run switch and then attn switch.

u. TTY prints:

TST 06

DEVICE ADDR. FORMAT

OUTPUT MODE = FXX1

INPUT MODE = FXXO

NO DEVICE = 0

LEVEL 2 DEVICE ADDR. =

v. Type in:

F800(C/R)

w. TTY prints :

INPUT MODE PRESS C/R

x. Press carriage return.

y. TTY prints :

TST 07

INPUT MODE PREPS C/R

z. Press carriage return.

aa. TTY prints :

TST 08

INPUT MODE PRESS C/R

ab. Press carriage return.

ac. TTY prints:

TST 09

INPUT MODE PRESS C/R

ad. Press carriage return,

ae. TTY prints:

TST 10

DEVICE ADDR. FORMAT:

OUTPUT MODE = FXX1

INPUT MODE = FXXO

NO DEVICE = 0

LEVEL 3 DEVICE ADDR. =

af. Type in:

O(C/R)

ag. TTY prints :

TST 14

TURN ON LINE FREQ. CLOCK,
PRESS ATTN.

ah. Set the LINE FREQ switch (S70), (located on bottom edge of Program Maintenance Panel) to ON and then press attn switch.

ai. TTY prints:

TST 15

TST 16

TST 17

TURN OFF LINE FREQ. CLOCK,
PRESS RUN

aj. Set the LINE FREQ switch (S70) to OFF and then press run switch.

ak. TTY prints:

TST 18

1110 CPU

al. Program halts.

am. Press reset switch and then load switch.

an. At ACOC Site, when tape motion halts, press switches 15 and 14 in data line and switch 2 in register line. Press the write switch in register line.

At Switch Site, when tape motion halts, press switches 15, 14, and 13 in data line and switch 2 in register line. Press write switch in register line; then press clear switch in address and data line.

ao. Press run switch.

ap. Number of test will appear in switches 0 through 3 of data line and loop count will appear in switches 4 through 15.

NOTE

At Switch Group only, complete steps aq through aw.

aq. Press halt switch: then press clear switch in data and address lines and repeat step an.

ar. Press switch 0 in data line and all switches in address line.

as. Press write switch in address line.

at. Press switch 9 (lamp on) and switch 0 (lamp off) in data line, and switch 0 in register line.

au. Press write switch in register line.

av. Press run switch and observe loop count in switches 4 through 15 of data line.

aw. Repeat steps aq through av twice, except in step ar press switch 1 in data line on first repeat and switches 1 and 0 on second repeat.

ax. At Switch Site, repeat steps am through aw twice. At ACOC Site repeat an through ap twice.

ay. Press reset s-witch and then load switch.

az. When tape motion halts, press run switch.

ba. TTY prints:

LF CLOCK/PWR FAIL TP

TURN ON LF CLOCK, PWR FAIL, PWR RESTART, PRESS RUN, ATTN

bb. Set the switches, located on bottom edge of Program Maintenance Panel, as follows:

1. LINE FREQ to ON
2. PWR RCVRY to IN
3. PWR FAIL to ON

bc. Press run and attn switches. After approximately 30 seconds, TTY prints:

TST 01

CLOCK COUNT = abcd

(where abcd is number of interrupts that occurred)

TTY prints:

TST 02

TURN POWER OFF/ON, PRESS ATTN

bd. Turn OFF, and then ON, AC POWER 120V switch on Multiple Power Supply 1, located below the Processor. Depress POWER ALARM RESET Switch on Alarm and Control Panel.

be. Press attn switch.

bf. TTY prints:

TST 03

TURN POWER OFF/ON, PRESS ATTN

bg. Repeat steps bd, be, and bf.

bh. TTY prints:

TST 04

TURN POWER OFF/ON, PRESS ATTN

bi. Repeat steps bd, be, and bf.

bj. Program halts.

bk. Press reset switch and then load switch.

bl. When tape motion halts, press run switch.

bm. TTY prints :

CONTROL PANEL TP

PANEL TYPE =

bn. Type in:

2200(C/R)

bo. TTY prints:

PANEL ADDR =

bp. Type in:

FF80(C/R)

bq. TTY prints :

TST 01

PRESS RESET, ATTN

br. Press reset switch and then attn switch.

bs. TTY prints :

TST 02

IF IDLE, PRESS RESET, ATTN
(ERROR NOT IDLE)

bt. Press reset switch and then attn switch.

bu. TTY prints the following and then halts:

TST 03

**DO THIS	**CHECK LITES**	
PRESS	ON	OFF
INH	IDLE, INH	
ATTN	IDLE, INH, ATTN	
ATTN	IDLE, INH	ATTN
HALT	HALT, INH	
INH	HALT	INH
RUN, ATTN		

bv. Perform each action listed under "DO THIS" and check that the lamps listed under ON are lighted and those listed under OFF are not lighted.

bw. TTY prints:

TST 04

TURN POWER ON/OFF KEY STRAIGHT UP

VERIFY ALL SWITCHES ON PANEL ARE LOCKED OUT

TURN POWER ON/OFF KEY TO RIGHT, PRESS ATTN

NOTE

Test 04 is not implemented in this system.

bx. Press attn switch.

by. TTY prints:

TST 05

VERIFY DATA ENTERED INTO ADDRESS/ENTRY

REG = DATA/RESPONSE REG

PRESS ATTN TO EXIT TEST

bz. Press switches 15, 13, 11, 9, 7, 5, 3, and 2 in address line and press write switch in address line. Press read s-witch in address line.

ca. Switches 15, 13, 11, 9, 7, 5, 3, and 2 are lighted in data line.

cb. Press attn switch.

cc. TTY prints :

TST 06

AT HALT, VERIFY FOLLOWING

R1 = 1111 R2 = 2222
R3 = 3333 R4 = 4444

R5 = 5555 R6 = 6666
R7 = 7777, PRESS RUN

cd. Press switch 1 and then the read switch in register line.

ce. Hexidecimal 1111 is displayed in data line.

cf. Repeat step cd six times using, in sequence, switches 2, 3, 4, 5, 6, and 7.

cg. Hexidecimal 2222, 3333, 4444, 5555, 6666, and 7777 are displayed in sequence in data line.

ch. Press run switch.

ci. TTY prints:

TST 07

PRESS ADH, ATTN

AT ADDRESS HALT VERIFY PC = abcd +-2, PRESS RESET, ATTN

(where abcd is a hexidecimal number)

cj. Press adh and then attn switches.

ck. Press switch 0 in register line.

cl. Press read switch in register line.

cm. Data line display is same as abcd +-2 of step ci.

cn. Press reset and then attn switches.

CO. Repeat steps ch through cm twice. The program supplies different values for abcd.

cp. TTY prints :

PRESS STEP SWITCH THREE TIMES

VERIFY PC = abcd PRESS RUN

(where abcd is a hexidecimal number)

cq. Press step switch three times.

cr. Press switch 0 in register line.

cs. Press read switch in register line.

ct. Data line display is same as abcd, +-2, of value in step cp.

cu. Press run switch.

CV. TTY prints:

TST 08

STORE RANDOW DATA IN ADDRESS > abcd PRESS ATTN

(where abcd is a hexidecimal number)

CW. Assume abcd = F800; store 1357 in F804 as follows:

Press switches 12, 9, 8, 6, 4, 2, 1 and 0 in data line. Press switches 15 through 11 and 2 in address line. Press write switch in address line and then press write switch in register line.

cx. Press attn switch.

cy. TTY prints:

TST 09

cz. Shifting patterns of 1s (ones) are displayed in address and data lines. After checking each pattern. program halts.

da. Press reset switch and the load switch.

db. When tape motion halts, press run switch.

dc. TTY prints:

TTY TEST′

TTY LEV=

dd. Type in:

2(C/R)

de. TTY prints :

TTY ADD =

df. Type in:

F80O(C/R) to test ASR-35 or KSR-35

F81O(C/R) to test RO-35

dg. TTY prints:

BTA = (YES = 1, NO = 0)

dh. Type in:

0(C/R)

di. TTY prints :

```
TST 01
TST 02
THE QUICK BROWN FOX SLYLY JUMPED OVER THE LAZY DOG.
TST 03
1"#$7.&'()*+,-./0123456739:;(=,?@ABCDEFGHIJKLMNOPQRSTUVWXYZ(\=)
'"#s%&'*+,-./O123456789:;=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\l)!
$%&'()*+,-/0123456789:;*-->?@ABCDEFGHIJKLMNOPQRSTUVWXYZ'(\)!#
          -./0123456739:;<--,?<?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\)  !"#
%&'()*+- ./0123456789:;<-,?@ABCDEFGHIJKLMNOPQRSSTUVWXYZ[\)!"#$
TST A3
TYPE ON KEYBOARD
```

NOTE

When an RO-35 is under test, lines 1, 2, 4, 10, and 11 above, are printed on KSR-35. This concludes the test for an RO-35.

dj. For a KSR-35 or ASR-35, type in:

F8C0

dk. TTY prints:

FF88CCOO

dl. Program should go to idle.

dm. Press reset switch and then load switch.

dn. When tape motion halts, depress ON LINE switch (lamp OFF) on Mag Tape Unit Al.

do. Depress REWIND switch.

dp. Tape rewinds and halts.

dq. Depress REWIND switch again to complete rewind sequence.

dr. Remove ATP test tape from Mag Tape Unit Al.

ds. Mount a blank tape (with write-enable ring) onto each mag tape drive. Thread the tapes following instructions on front panel of tape transports.

dt. Depress LOAD switch on Mag Tape Unit Al.

du. When tape motion halts, depress LOAD switch again.

dv. Depress ON LINE switch (lamp lights).

dw. Repeat steps dt, du and dv for Mag Tape Unit Al.

dx. Press run switch on Program Maintenance Panel.

dy. TTY prints :

SUE MAG TAPE (BTA) TP

R/R OR C (1 OR 0) =

dz. Type in:

1(C/R)

ea. TTY prints:

ADDR =

eb. Type in:

F8CO(C/R)

ec. TTY prints :

LVL =

ed. Type in:

3(C/R)

ee. TTY prints:

DRIVES =

ef. Type in:

2(C/R)

eg. TTY prints :

RD/WRT OR WRT (1 OR 0) =

eh. Type in:

1(C/R)

ei. TTY prints:

SET DRV SLCT UNIT O=O, ETC, PRS RUN

ej. Press run switch.

ek. TTY prints:

DFN TST PRMTRS (1 OR 0) =

el. Type in:

0(C/R)

em. TTY prints:

RCDS =

en. Type in:

20(C/R)

eo. TTY prints:

WRDS =

ep. Type in:

5(C/R)

eq. TTY prints:

DATA =

er. Type in:

A55A(C/R)

es. TTY prints:

RWND & LV ALL UNITS ON LINE, LOAD, WRT EN, PRS RUN

et. Press run switch.

eu. TTY prints:

TST 01

** UNIT 0

** UNIT 1

** UNIT 0

TST 02

TST 03

TST 04

TST 05

TST 06

TST 07

TST 08

TST 09

TST 10

TST 11

** UNIT 1

TST 02

TST 03

TST 04

TST 05

TST 06

TST 07

TST 08

TST 09

TST 10

TST 11

END OF TEST LP CT=0001

ev. Press halt switch, This concludes ATP test.

6-96. RESTORING CORE MEMORY

6-97. After performing the test checks of paragraph 6-94, restore Core Memory program as described in paragraph 6-16.

ALPHABETICAL INDEX

ALPHABETICAL INDEX (cont)

ALPHABETICAL INDEX (cont)

CROSS-REFERENCE INDEX

(Prefix each Reference Number with the Chapter Number denoted by the Column.)

(KEY: Numbers preceded by "f" are illustrations: "t" are tables; others are paragraphs.)

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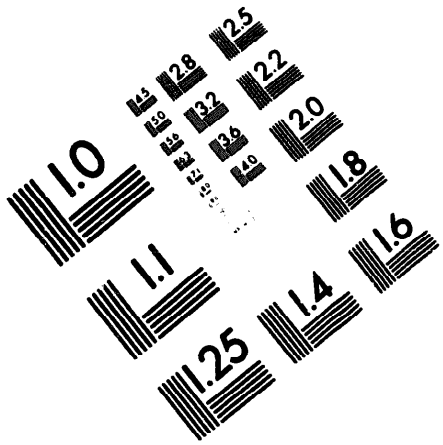
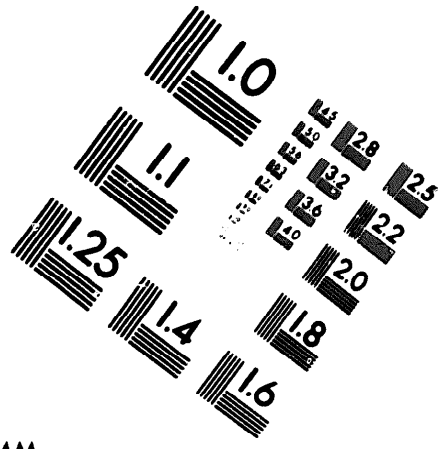
END

11-10-82

DATE

TEST TARGET





150 MM

1.0 mm (e= .81 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

1.5 mm (e= 1.09 mm)

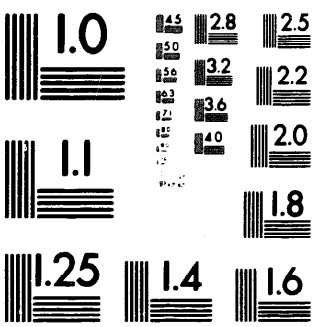
ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

2.0 mm (e= 1.37 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

2.5 mm (e= 1.77 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*



1.0 mm (e= .81 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

1.5 mm (e= 1.09 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

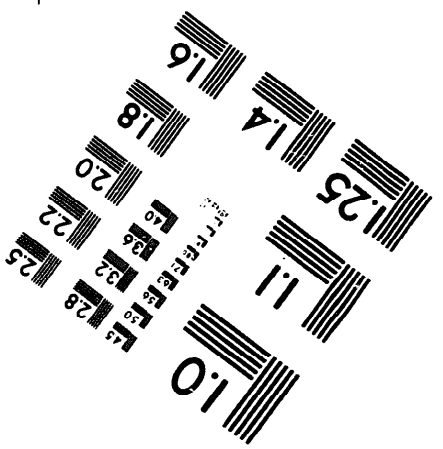
2.0 mm (e= 1.37 mm)

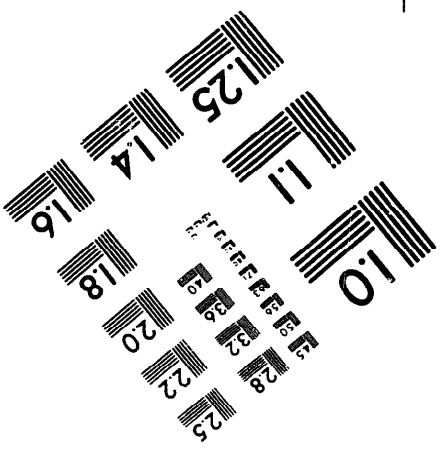
ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

2.5 mm (e= 1.77 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

200 MM





250 MM